Vol. 5 • Issue 1

2023

Signal Integrity Journal™

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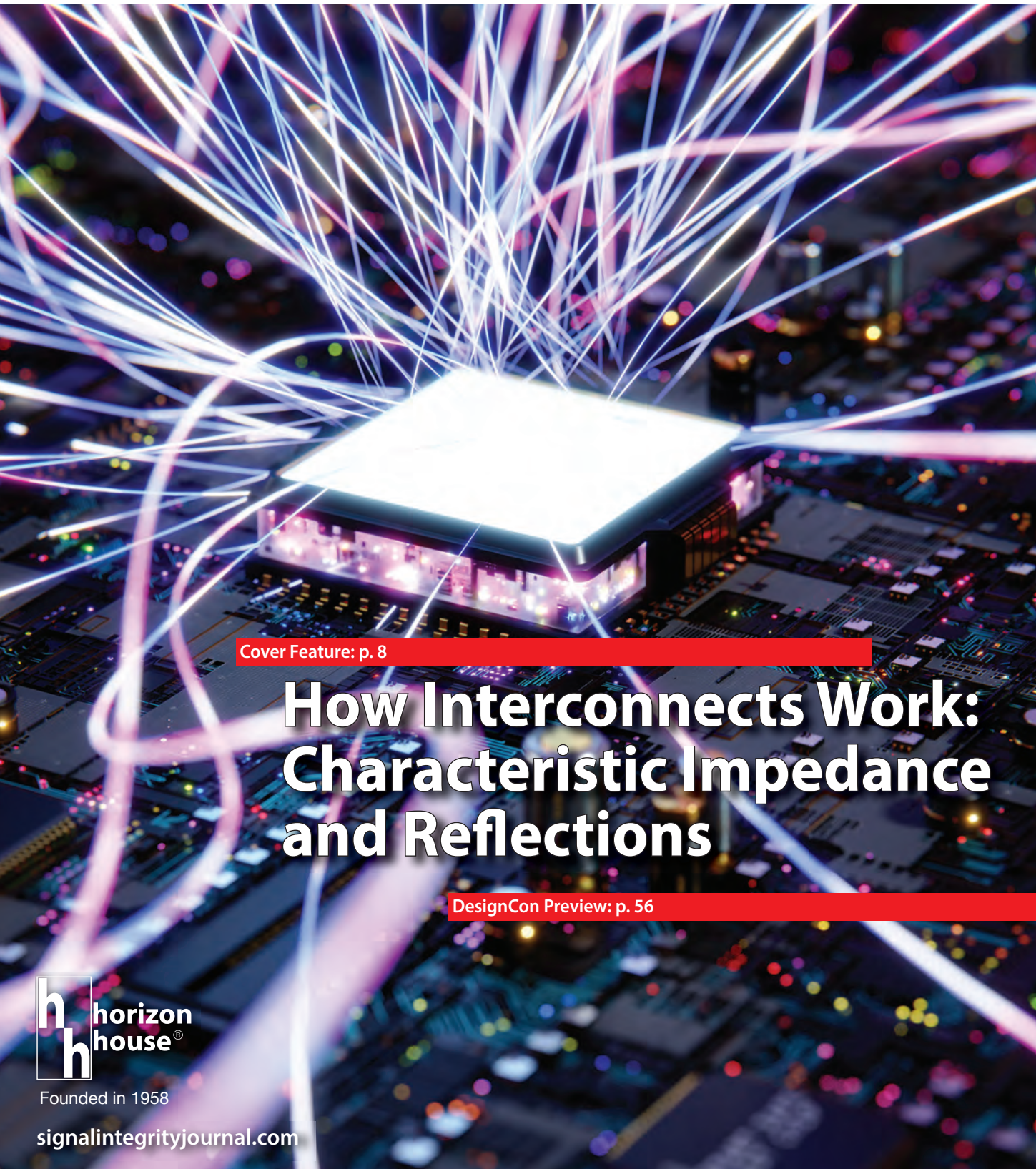

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A National Security Crisis the Industry Can Address

Eric Bogatin, Technical Editor
Signal Integrity Journal

Not a week goes by that I do not get an email from a colleague in the industry wanting to hire a recent graduate with experience in signal integrity. Even in an economic downturn, there are more openings for qualified signal integrity engineers than there are current engineers, or recent graduates.

I define signal integrity as a problem which arises when interconnects are not transparent. This means their design influences the noise in an electronic product. When interconnects are not transparent to signals, they have the potential of creating noise and preventing a product from meeting specifications, unless special care is taken in their design.

In almost all products today, interconnects are not transparent. Even in an IoT application, with a 16 MHz clock, switching noise, ground bounce, and EMI may cause a product to fail if the interconnects are not designed with signal integrity in mind. This is why I always say, "there are two kinds of engineers, those who have signal integrity problems, and those who will."

The gap between the demand in the industry and the supply of engineers with signal integrity design skills is widening. This problem is even more critical in the U.S. defense industry where most engineers must be International Traffic in Arms Regulations (ITAR) compliant. This means they must be U.S. citizens or permanent residents with Green Card status. According to the IEEE, the percentage of Ph.D. or M.S. graduates in electrical engineering awarded from U.S. universities who are U.S. citizens is currently less than 30% and has steadily declined since about 2005.

The demand is growing, and the supply of ITAR qualified engineers is declining. This is a national security crisis. As an industry, there are two things we can do to have an impact on this growing crisis.

First, vendors with tools used in signal integrity design or analysis can provide free "student" versions to give both enrolled students and engineers looking to grow their skills, an opportunity to learn by doing. Some large EDA companies such as Ansys, Keysight, and Altium already do this. Rather than cannibalizing the sale of a full seat, these free versions capture mind share and give engineers a taste of the user interface and the capabilities of the tools. Guaranteed, every student learning to use one of these platforms from the student version will be a future user of EDA tools. When they are in a position to influence a purchase, which tools do you think they will recommend?

This goes for hardware as well. Most instruments, such as scopes, VNAs, TDRs, and signal generators are basically computers with some data acquisition analog front or back ends. When it is appropriate, the user interface software can be offered for free to students to practice measurement analysis.

Some scope vendors such as Teledyne LeCroy, Keysight, and Tektronix already do this. Live scope measurements can be recorded, saved in a proprietary format, and uploaded into these "virtual" instruments to be viewed and analyzed, as though they were just recorded. This gives students a taste of the experience of performing a measurement and analyzing the result.

Some scope vendors, such as Digilent, even allow the free version of their scope's user interface to collect live measurements from a PC sound card input so a student can learn the user interface on real measurements. The next step is to integrate any data streamed over a serial port, such as from a microcontroller's output, into the scope's user interface. This would give the students a real-time signal to explore.

Of course, there is no substitute for actual hands-on experience with a real instrument. Hardware tool vendors should consider the option of donating hardware to schools and universities to capture mind share of students and give them exposure to real measurements and inspire them to pursue a hardware engineering path.

The second action industry can take to create more U.S. citizen engineers with experience in signal integrity is to offer scholarships for both undergraduate and graduate degrees. Support and invest in your current employees' growth as an engineer by encouraging them to take a class or pursue a degree in a specialized field. A few universities, such as Penn State, Missouri University of Science and Technology, and University of Colorado, Boulder, offer advanced degrees with a focus on signal integrity.

To grow new engineers, hire a college sophomore as an intern. If they show promise, offer them a scholarship if they pursue a hardware-related degree and bring them back for summers. Supporting and encouraging young engineers will capture their mind share and inspire them to pursue a field that will help keep our industry and economy strong.

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How Interconnects Work: Characteristic Impedance and Reflections

Yuriy Shlepnev
Simberian Inc., Venice, Calif.

Digital interconnects are modeled as transmission lines defined by characteristic impedance and propagation constant. This article explains how transmission lines work and provides practical formulas for investigation of signal degradation due to absorption and reflections losses. Optimal characteristic impedance is defined for printed circuit board (PCB) and packaging interconnects as the impedance that minimizes the power absorbed by interconnects and terminators. It is shown that 50Ω single-ended or 100Ω differential may be not optimal if we need either longer reach or spend less energy per bit transmitted over interconnects.

Analysis of "digital interconnects" is the analog problem in frequency domain where interconnects are simulated as transmission lines defined by characteristic impedance and propagation constant. Digital signals in interconnects are sequences of amplitude-modulated pulses that transmit bits between components. The "digital interconnect" analysis problem is technically an analog problem of pulse propagation modeling in time domain. Sequence of the transmitted bits (1 s and 0 s) is the only boundary between the digital and the analog interconnect analysis domains. Though, that time domain analysis problem is almost always solved in the frequency domain. A pulse or sequence of pulses are transformed into a superposition of harmonics or sinusoidal signals in time domain because it is mathematically easier and more convenient to model all types of signal degradation for the harmonic signals using phasors and complex analysis.[1] Components on PCBs in the digital domain are just connected—1 s and 0 s are supposed to flow seamlessly between the components. In the analog or RF/microwave domain, components on PCBs or in a package are connected with distributed open waveguiding structures composed of traces and reference conductors and simulated mostly as transmission lines. To ensure that the digital signal is actually getting through, we have to

build interconnect models that include all signal degradation factors important for a specific data rate.

In general, all signal degradation factors can be separated into three categories:

- Absorption losses in dielectrics and conductors
- Reflection losses due to impedance mismatch and discontinuities
- Coupling losses and distortion (includes crosstalk).

The absorption or dissipation losses in dielectrics and conductors were recently discussed in a previous article.[2] Such losses are inevitable but can be effectively mitigated at the stackup planning stage—selection of dielectric and conductor materials and stackup geometry defines the maximum possible communication distance for a particular data rate.

Considering the reflections, they can be further separated into the following three categories:

- Reflections from transmission lines and termination impedance mismatch
- Reflections from single discontinuities—vias, transitions, AC caps, gaps in reference plane, etc.
- Reflections from periodic discontinuities—cut outs, fiber-weave effect, etc.

Why do we care about the reflections?—Because reflections degrade the transmitted signal, and such degradation may cause link failure. Thus, understanding and evaluation of reflections is useful for channel quality control and there are corresponding compliance metrics in frequency domain (bounds on reflection loss) as well as in time domain (effective return loss).

Here we will take a closer look at the reflections caused by the transmission line characteristic impedance and termination impedance mismatch. We have discussed it in our "Design Insights…" tutorial at the last "normal" DesignCon in 2020 and this paper is loosely based on that.[3]

Transmission Line Theory

Impedance and admittance as well as impedivity, admittivity, conductivity, succeptance, leakance, voltivity, and gaussivity are the terms introduced by Oliver Heaviside at the end of 19th century during the golden era of electromagnetic discoveries started by James Clerk Maxwell. Heaviside derived the Telegrapher's equations describing transmission lines or, as we know now, any waveguiding system in general. The equations describe one-dimensional distributed problem that for a two-conductor or one-mode (one signal and one reference conductor) transmission line looks as follows:

$$\frac{\partial V(x)}{\partial x} = -Z(f)\cdot I(x) \qquad Z(f) = R(f) + i2\pi f \cdot L(f)$$

$$\frac{\partial I(x)}{\partial x} = -Y(f)\cdot V(x) \qquad Y(f) = G(f) + i2\pi f \cdot C(f)$$

Where I is the current, V is voltage changing along the x-axis, f is frequency (Hz). Z (Ω/m) is complex impedance per unit length and Y (S/m) is complex admittance per unit length, R (Ω/m) and L (Hn/m)—are real frequency-dependent resistance and inductance per unit length, G (S/m) and C (F/m)—are real frequency-dependent conductance and capacitance per unit length. Z, Y, R, L, G, and C for N+1 conductor problem or N-mode transmission line are NxN matrices in general. They are 2×2 matrices for a three-conductor differential line for instance. The impedance and admittance per unit length are frequency-dependent, in general, and are completely defined by transmission line type and cross-section and usually computed either with a static or quasi-static 2D field solver or sometimes with 3D EM solvers. Note that the use of 3D solvers does not automatically guarantee higher accuracy.

A solution of the Telegrapher's equation can be written as a superposition of two waves propagating in opposite directions as follows (can be easily verified by inspection):

$$V(x) = v^{+}\cdot\exp(-\Gamma\cdot x) + v^{-}\cdot\exp(\Gamma\cdot x)$$

$$I(x) = \frac{1}{Z_c}\left[v^{+}\cdot\exp(-\Gamma\cdot x) - v^{-}\cdot\exp(\Gamma\cdot x)\right]$$

$$\Gamma(f) = \sqrt{Z(f)\cdot Y(f)} = \alpha(f) + i\beta(f)$$

$$Z_c(f) = \sqrt{Z(f)/Y(f)}$$

Where Z_c is complex frequency-dependent characteristic impedance and gamma is complex propagation constant (α is the attenuation constant (Np/m) and beta is the phase constant (rad/m) defined as $2\pi/\lambda$, Lambda is the wavelength in the transmission line—phase changes by 2π over that length, see more in the Appendix). Those are the modal parameters in general—the equations above are for a two-conductor line with one mode only. If we write the solution for the wave propagating only in one direction along the x-axis for instance (would be ideal for signal transmission):

$$v(x) = v^{+}\cdot\exp(-\Gamma\cdot x), \quad i(x) = \frac{v^{+}}{Z_c}\exp(-\Gamma\cdot x)$$

We can see that the characteristic impedance is just a ratio of the voltage and current of the wave propagating in one direction of transmission line $v(x)/i(x)=Z_c$. It is impedance by dimension (Ω). It is pure resistance if line is lossless. The word "characteristic" is used because it does not depend on the position or length of transmission line segment (independent of x)—it "characterizes" it. It depends only on the type of transmission line and geometry of the cross-section. Note that for planar transmission lines, used for PCB and packaging interconnects, the definition of impedance is not unique and can be done in three ways—through voltage and current, current and power, and voltage and power, but they all close to the conventional "static" voltage-current definition if cross-section remains much smaller than the wavelength, which is usually good assumption for PCB and packaging interconnects.

To investigate the reflections, the next step is to define the properties of a transmission line segment. The Telegrapher's equations introduced in the previous section are incomplete without the "boundary conditions" or terminations. The most effective way to describe a segment is to use waves and scattering parameters (S-parameters). Here is a transmission line segment with length l connected to voltage sources with all variables,

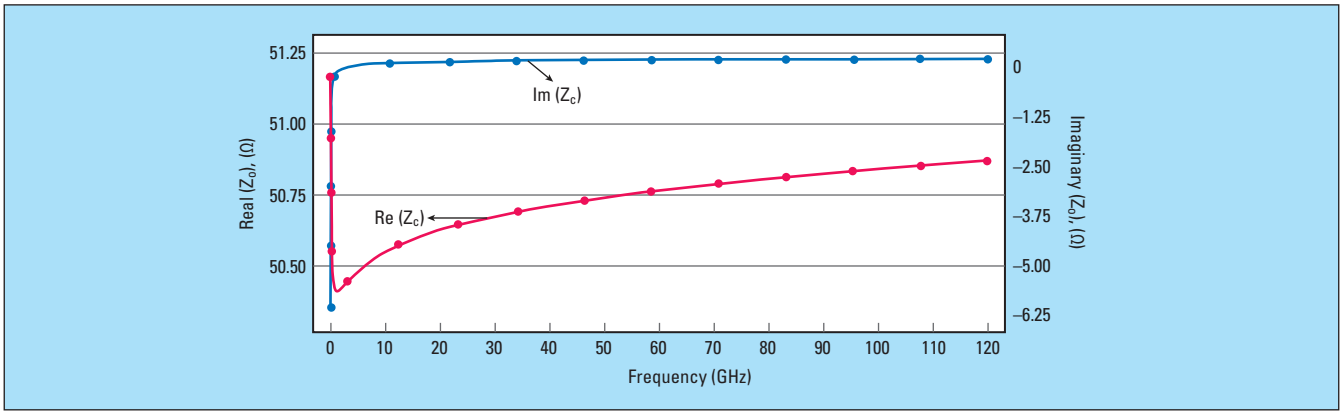

Fig. 1 Characteristic impedance is complex for lossy lines showing imaginary and real parts.

to define S-parameters:

$$S_{i,j}=\left.\frac{b_i}{a_j}\right|_{a_k=0,k\neq j}$$

Incident Waves: $a_1=\frac{1}{2\sqrt{Z_0}}(V_1+Z_0\cdot I_1)$ $a_2=\frac{1}{2\sqrt{Z_0}}(V_2+Z_0\cdot I_2)$

Reflected Waves: $b_1=\frac{1}{2\sqrt{Z_0}}(V_1-Z_0\cdot I_1)$ $b_2=\frac{1}{2\sqrt{Z_0}}(V_2-Z_0\cdot I_2)$

Where a_1, a_2 are the "incident waves," and b_1, b_2 are the "reflected waves" with dimension sqrt (Wt). V_1, V_2 and I_1, I_2 are voltages and currents at the segment ports (pairs of terminals). Z_0 is the termination or normalization impedance (same thing in this context). Waves in this definition are not actual waves in the transmission line, but rather variables formally defined through voltage and current. Using equations for voltage and current in the transmission line segment (superposition of two waves defined earlier) and Kirchhoff's laws at the external terminals or by following more formal procedure from "S-parameters for Signal Integrity,"[4] we can define S-parameters or S-matrix that relates the incident and reflected waves for such segment as follows:

$$S(f,l)=\begin{bmatrix}\left(Z_c^2-Z_0^2\right)/D & 2\cdot Z_c\cdot Z_0\cdot csh(\Gamma\cdot l)/D\\ 2\cdot Z_c\cdot Z_0\cdot csh(\Gamma\cdot l)/D & \left(Z_c^2-Z_0^2\right)/D\end{bmatrix}$$

$$D=Z_c^2+Z_0^2+2\cdot Z_c\cdot Z_0\cdot cth(\Gamma\cdot l)$$

The reflection (S11 and S22) and transmission (S12 and S21) can be expressed separately as follows:

$$S_{1,1}=S_{2,2}=\left(Z_c^2-Z_0^2\right)/\left(Z_c^2+Z_0^2+2\cdot Z_c\cdot Z_0\cdot cth(\Gamma\cdot l)\right)$$

$$S_{1,2}=S_{2,1}=2\cdot Z_c\cdot Z_0\cdot csh(\Gamma\cdot l)/\left(Z_c^2+Z_0^2+2\cdot Z_c\cdot Z_0\cdot cth(\Gamma\cdot l)\right)$$

Note that the transmission parameters include the effects of absorption and reflections—there are no approximations in these expressions. This is a universal definition of the reflection and transmission—it can be used for simple experiments with transmission line properties or as rigorous modelling of a segment. It depends on the definition of characteristic impedance and propagation constant used. The rest is pure trigonometry. You can start with a frequency-independent capacitance and inductance per unit length or use more complicated expressions for the characteristic impedance and propagation constant.[5] For simple experiments, the propagation constant can be defined analytically with formulas or simply with phase delay or propagation velocity for ideal lines (see Appendix). This is a simple and important tool for all kinds of experiments in the frequency domain with real transmission lines. It includes all reflections in time domain (if model bandwidth is properly defined).[1] Though, use of frequency domain response for time domain analysis is not as easy.[4] Simbeor software is used here for all frequency and time domain analyses—it makes our investigation easier.

Now, what useful information can be derived from such a simple trigonometric model? Let's begin from a very simple case of the termination or normalization impedance equal to the characteristic impedance $Z_0=Z_c$—the reflection parameter is zero in this case as we can see from the formula. The S-matrix in this case is simple and defined as follows (generalized modal S-parameters):

$$S(f,l)=\begin{bmatrix}0 & \exp(-\Gamma\cdot l)\\ \exp(-\Gamma\cdot l) & 0\end{bmatrix}$$

Only the transmission parameters and no reflections—this should be the Holy Grail of the interconnect design—the signal is travelling strictly in one direction. Though, the signal may still not get through because the transmission parameter depends on the absorption and dispersion in Gamma discussed earlier.[2] Considering the zero-reflection condition, why do we not do it like that way? First, the characteristic impedance is complex for lossy lines—it has real and imaginary parts. The zero-reflection termination is not just a resistor—it should be frequency dependent. But this is not the showstopper—the real part of the characteristic impedance does not change much at the important frequencies and the imaginary part is much smaller than the real part, as can be seen in ***Figure 1*** (typical PCB case).

So, at least theoretically, we should be able to get very close to the non-reflective case. Practically, there are more factors that do not allow this to happen—the manufacturing variations and discontinuities such as pads and viaholes are the most important ones.

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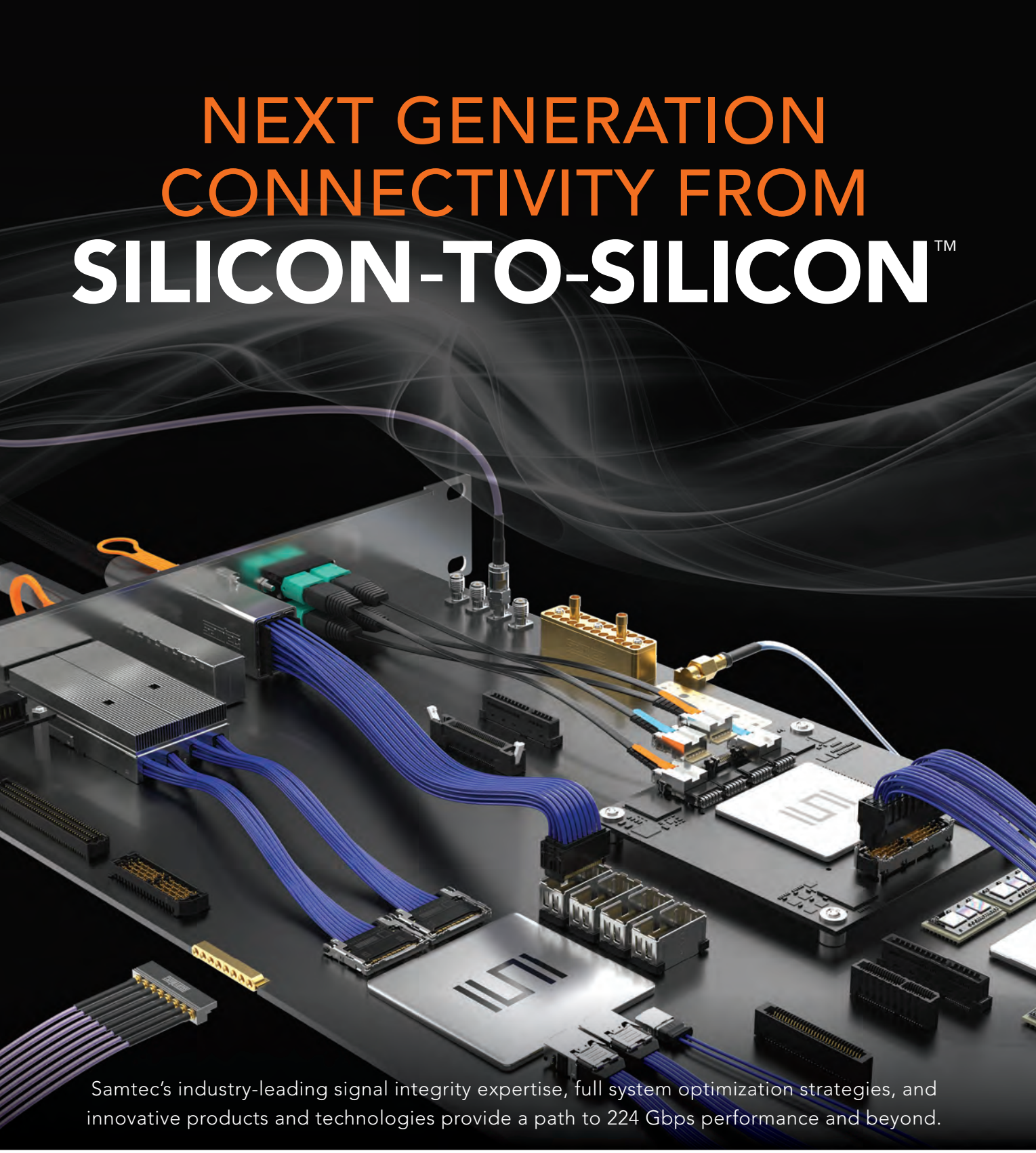

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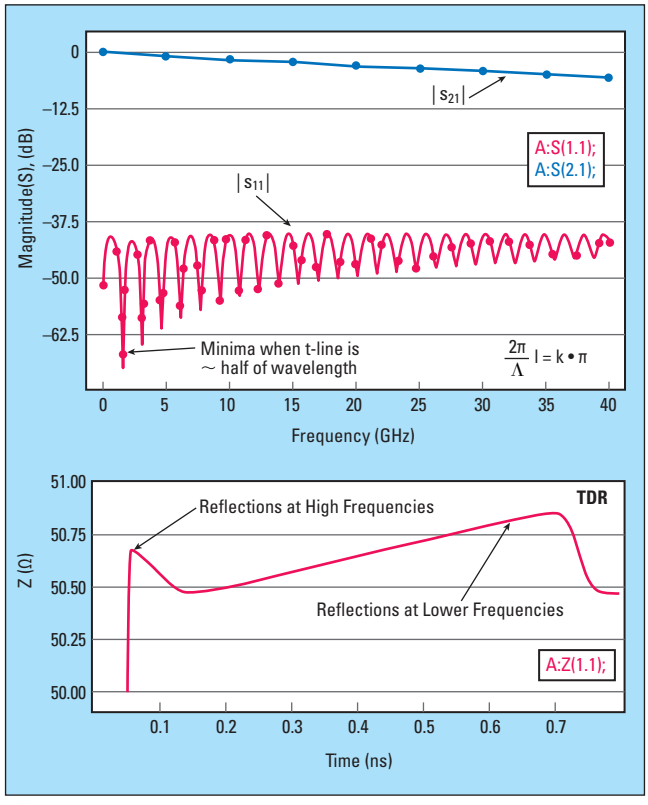

Fig. 2 5 cm transmission line segment simulated response in frequency and time domains terminated at 50Ω (computed with Simbeor software).

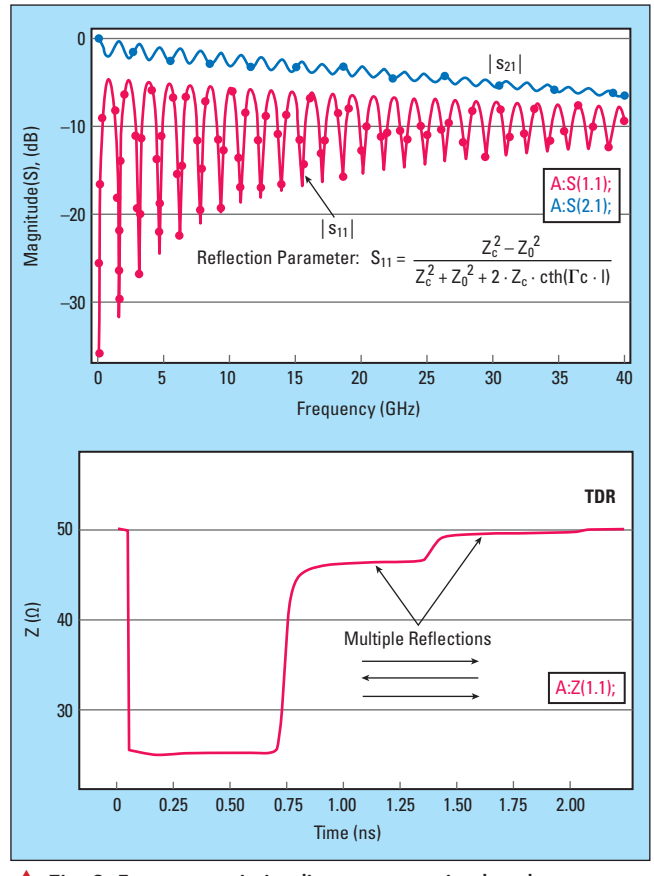

Fig. 3 5 cm transmission line segment simulated response in frequency and time domains terminated at about 25Ω (computed with Simbeor software).

Transmission Line Segment Example

Now, armed with the theory, let's investigate a simple 5 cm stripline segment with characteristic impedance about 50.4Ω at 1 GHz (changing with frequency as shown above) on FR408 simulated as Wideband Debye with Dk=3.8, LT=0.0117 at 1 GHz, copper with RR=1.2, Causal Hammerstad Roughness Model: SR=0.4, RF=2. This situation is realistic, and the only simplification is the absence of the discontinuities. The transmission line segment has the response in frequency and time domains shown in ***Figure 2***.

Both ends of the transmission line segment are terminated by 50Ω (exactly). Magnitudes of the reflection |S11| and transmission |S21| parameters are shown on the top plot and corresponding TDR on the bottom plot (reflection from 20 ps step response in ohm). S-parameters are shown in dB (20log(|S11|) and 20log(|S21|)). First, we can observe that the reflection is not zero, but very low—below -37.5 dB (only about 13 mV is reflected with 1 V excitation—it is as good as it gets and usually not possible). Consequently, the transmission parameter magnitude is smooth and is defined mostly by the absorption by dielectric and conductors. Notice that the reflection parameter has some minima and maxima. The first maximum is at frequency where segment length is about equal to a quarter of wavelength in transmission line, defined by Gamma (see Appendix) and repeating every half of wavelength. The first minimum is at about half of wavelength is also repeated every half of the wavelength and explained next. The value of the reflection at one frequency point may be misleading. Considering the TDR, we can see that it shows some variations consistent with the variations of characteristic impedance.[6]

What if the characteristic impedance of the transmission line is significantly different from the termination impedance? Let's take a look at a 25 Ω stripline in the same stackup as before, shown in ***Figure 3***.

Magnitudes of the transmission (insertion loss) and reflection in dB are shown on the top plot and TDR on the bottom. The reflection went up considerably, that means more signal energy is reflected. As the result, the transmission or insertion losses went down at some frequencies—less signal energy is transmitted. The insertion loss now is wavy and repeats the reflection pattern—maxima in the reflection are the minima in the insertion losses. The signal energy here is either reflected or absorbed. The top plot also has the expression for the reflection parameter—the hyperbolic tangent in the denominator explains the minima and maxima—it is trigonometry, though with the complex numbers. S-parameters are used directly to compute the TDR that shows some multiple reflections from the ends of the segment in this case.

Another case with considerably larger characteristic impedance about 75Ω (cannot be exact) and same segment length and 50Ω terminations is shown in ***Figure 4***. The S-parameter plot looks very similar to the previous 25Ω case. Though, it has more conductive losses and the TDR goes up, instead of down, and shows more

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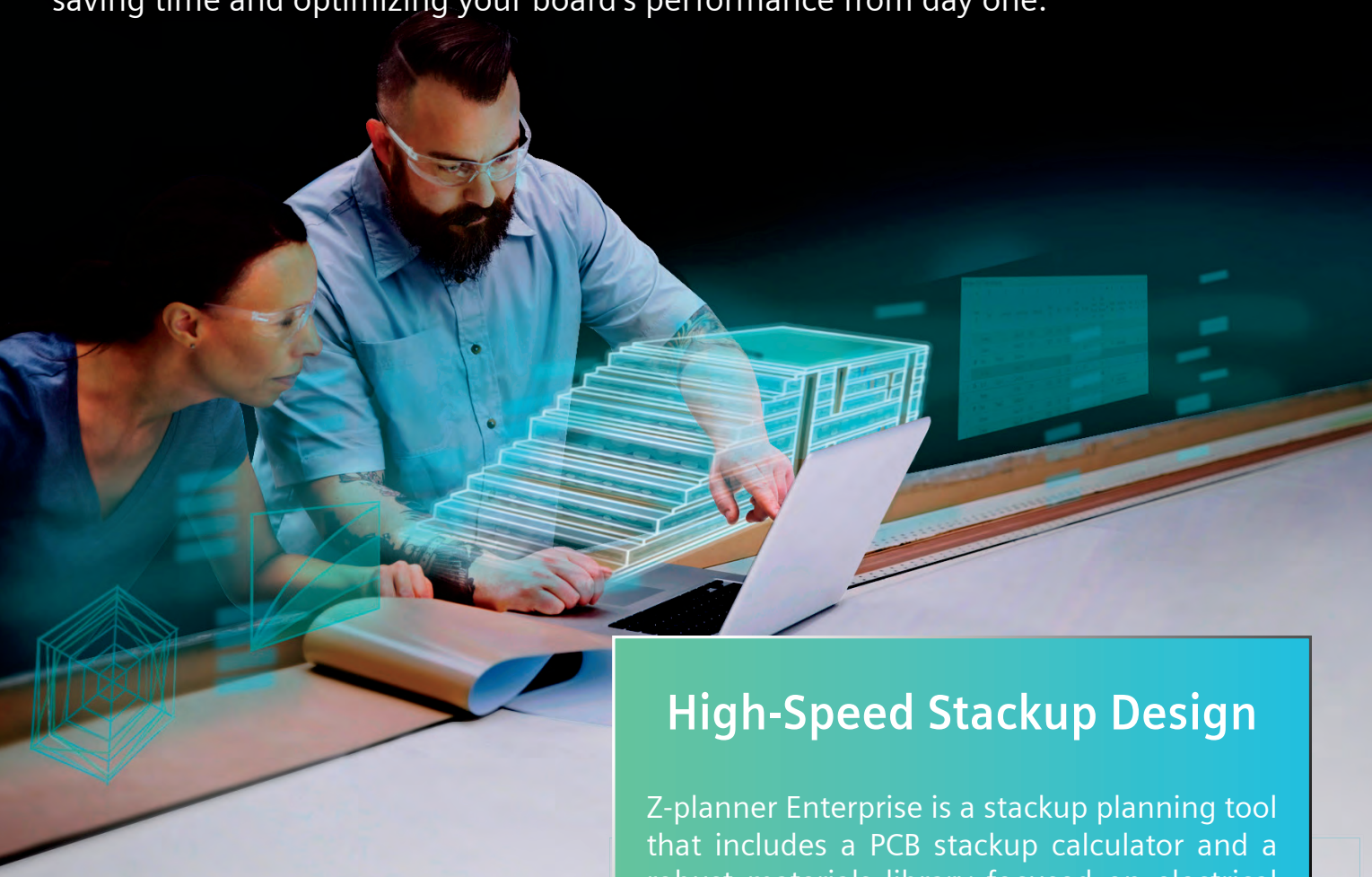

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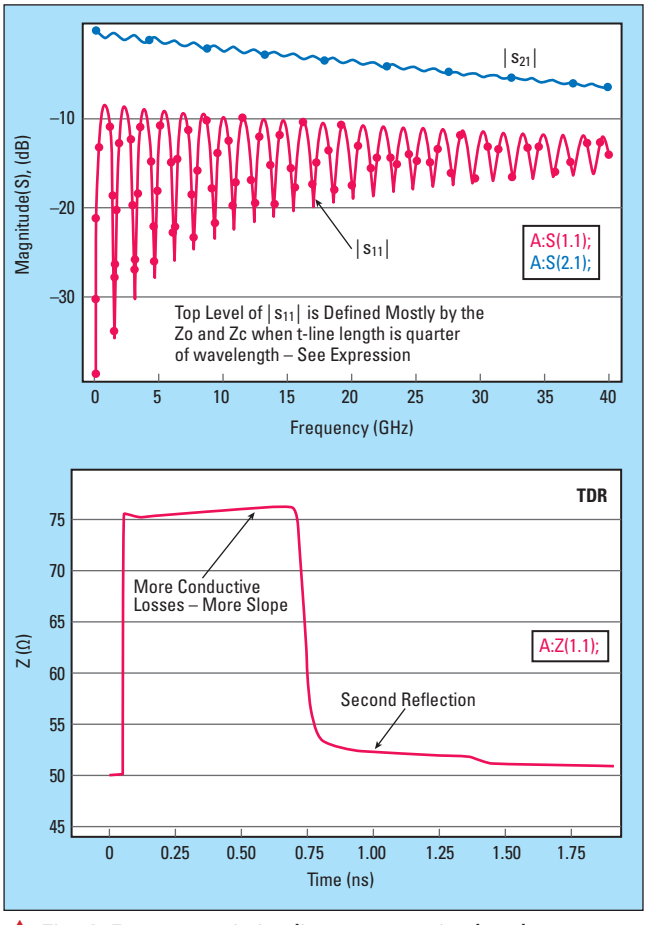
resistance (slope up) in the narrow transmission line as expected. In both "reflective" cases only one or two reflections are significant – it disappears quickly due to the absorption losses (losses are our friend in such reflective cases).

Optimal Characteristic Impedance

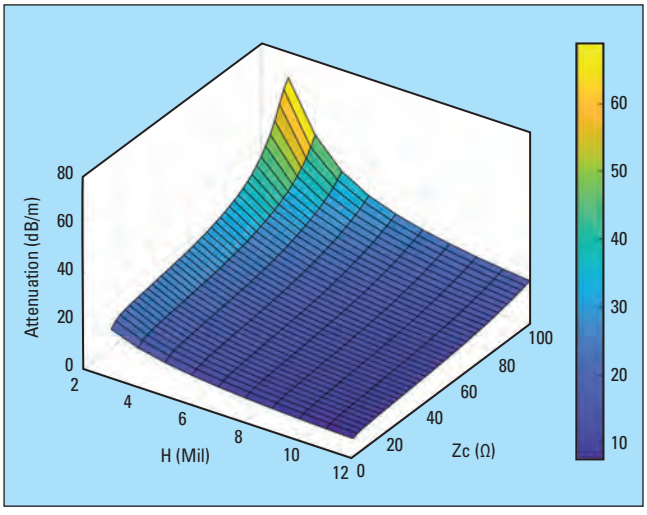
If you are wondering why characteristic impedance of 50Ω is usually selected for single-ended and 100Ω for differential PCB or packaging interconnects, you are not alone. It can only be explained by the historic reasons and convention for the component terminators. In fact, there are no reasons to stick with this number. As the story goes, 50Ω was the tradeoff impedance of an air-filled coaxial transmission line between the maximal transmitted power and minimal losses.[7] Indeed, a coaxial line always has a minimum in losses vs. impedance. Though it is dependent on the dielectric fill, but it happens to be close to 50Ω for coaxial lines filled with PFTE-type dielectric with Dk close to 2.[7] As we know, striplines are the descendants of the coaxial transmission lines, but the stripline losses do not have minimum on the loss versus impedance function. Here is the attenuation in dB/m for a stripline modeled with Dk=3.5, LT = 0.002 at 1.0e9, Huray-Braken roughness model: SR = 0.1 μm, RF = 9 as a function of dielectric thickness and characteristic impedance at 10 GHz, shown in ***Figure 5***.



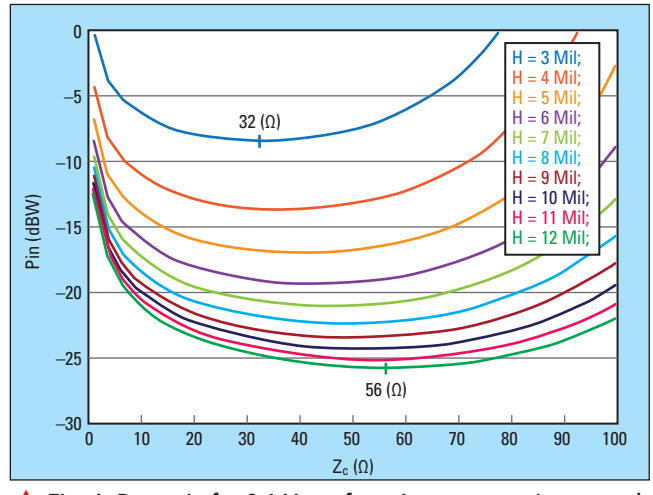
▲ Fig. 4 5 cm transmission line segment simulated response in frequency and time domains terminated at about 75Ω (computed with Simbeor software).

The attenuation is lower for the lower characteristic impedance (Z_c axis) as well as for the thicker dielectrics (H axis). The conductor losses dominate in striplines with very low loss dielectrics.[2] It means that the cross-sections with more metal and lower impedance have smaller losses in general. Though, the single mode propagation condition and layout density may put additional bounds on the increase of the cross-section size and on the lowest impedance as well. So, is the lower impedance always better? Not really, if our goal is to minimize the power absorbed by the interconnects and terminators. For instance, if we need 0.1 V signal at the receiver and compute power required at the transmitter side (Pin=20log(Vout)-10log(|Zc|)+Att_dB*Length, dBW), we will see some minima (same example as above at 10 GHz) as shown in ***Figure 6***.

The minimal power depends on the geometry (dielectric thickness H above and below trace and trace width adjusted to have an impedance value on the x-axis) and also on length (plots are for a 1 m segment). Lower impedance should be considered for thinner dielectric layers. Strip widths in this example are set to have the impedance shown on the x-axis (Simbeor SDK used for computations). Terminations in this case were set equal



▲ Fig. 5 Attenuation versus impedance at 10 GHz for a stripline (computed with Simbeor SDK for Matlab).



▲ Fig. 6 Power in for 0.1 V out for a 1 m segment (computed with Simbeor SDK for Matlab).

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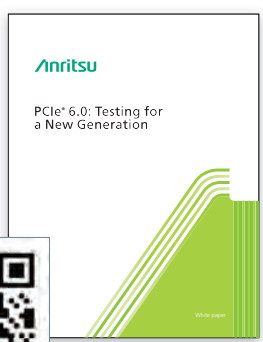

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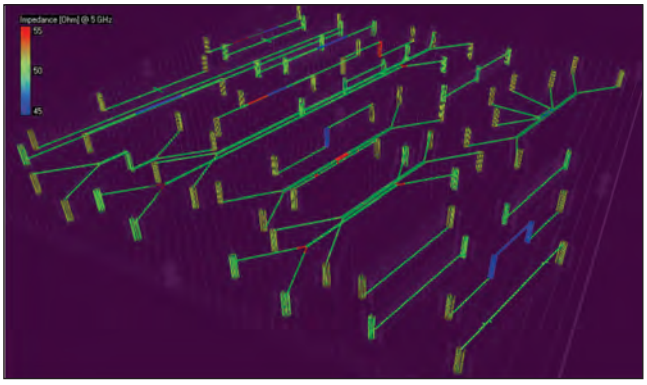

Fig. 7 Example of an impedance verification for CMP-28 validation platform from Wild River Technology in Simbeor 2022.02.

to the magnitude of the characteristic impedance at 10 GHz (no reflections). As we can see, the lower characteristic impedance is not always better and may be optimized for a particular system.

PCB Interconnect Example

Finally, the constant impedance from component to component should be the design goal, but it is usually violated in practical cases. The single-ended or differential traces are the open waveguiding structures composed of traces and reference conductors. Though, almost all layout tools do not take this into consideration. Thus, before any type of interconnect analysis, the impedance continuity should be verified first with a validated field solver. Shown in ***Figure 7*** is an example of such impedance verification for CMP-28 validation platform from Wild River Technology in Simbeor 2022.02.

The green color is used for objects with the impedance close to the target impedance (50Ω single-ended or 100Ω differential). Objects with the impedance below the target are blue and with higher impedances are red. This is a well designed board with a small number of intentional impedance violations in some structures. Also, it comes from Wild River Technology with the measurements up to 50 GHz for validation purposes. Simbeor evaluates the input impedance of the vias with fast EM models of multi-vias (signal + stitching vias) and impedance of traces with Simbeor SFS 2D field solver at the Nyquist frequency.

Another example of how the reference conductors can change the impedance of traces on a design with traces going through BGA breakouts is shown in ***Figure 8***. Here Simbeor evaluated effect of the cut-outs and reference pads on the impedance—those cannot be avoided. We can see that the impedance of connector and AC coupling pads is below the target and the impedance of the length compensation sections are above the target (layout mistake). The discontinuities in the reference conductors also create impedance violations (another layout mistake). Though, most of those violations may not kill the signal and are important at relatively high data rates.■

REFERENCES

1. Y. Shlepnev, "How Interconnects Work: Bandwidth for Modeling and Measurements," *Simberian App Note #2021_09*, November 8, 2021.
2. Y. Shlepnev, "How Interconnects Work: Absorption, Dissipation and Dispersion," *Simberian App Note #2021_10*, November 26, 2021.
3. Y. Shlepnev and V. Heyfitch, "Tutorial – Design Insights from Electromagnetic Analysis & Measurements of PCB & Packaging Interconnects Operating at 6- to 112-Gbps & Beyond," *DesignCon*, January 2020.
4. P. J. Pupalaikis, "S-parameters for Signal Integrity," *Cambridge University Press*, 2020.
5. "Can Conductor Roughness Effect be Accounted for in Dielectric Model?," *Simberian App Note #2012_02, 2012*.
6. "Micro-strip Line Characteristic Impedance and TDR," *Simberian App Note #2009_04, 2009.*
7. *"Why Fifty Ohms?," Microwaves 101, Web: https://www.microwaves101.com/encyclopedias/why-fifty-ohms.*

Appendix

Other useful transmission line modal parameters derived from the complex propagation constant (Gamma) and useful for understanding of transmission line behavior (omega is the radial frequency [rad/s]):

$$\Gamma_n(\omega) = \sqrt{z_{n,n}(\omega)\cdot y_{n,n}(\omega)} = \alpha_n + i\beta_n$$

$\alpha = \mathrm{Re}(\Gamma)$ attenuation constant [Np/m]

$\alpha_{dB} = \frac{20\cdot\alpha}{\ln(10)} \approx 8.686\cdot\alpha$ attenuation constant [dB/m]

$\beta = \mathrm{Im}(\Gamma)$ phase constant [rad/m]

$\Lambda = \frac{2\pi}{\beta}$ wavelength [m]

$\varepsilon_{eff} = \mathrm{Re}\left[-\left(\frac{c\cdot\Gamma}{\omega}\right)^2\right]$ effective dielectric constant

$p = \frac{c}{v_p} = \frac{c\cdot\beta}{\omega}$ slow-down factor, c is the speed of electromagnetic waves in vacuum

$v_p = \frac{\omega}{\beta}$ phase velocity [m/sec]

$\tau_p = \frac{\beta}{\omega}$ phase delay [sec/m]

$v_g = \frac{\partial\omega}{\partial\beta}$ group velocity [m/sec]

$\tau_g = \frac{\partial\beta}{\partial\omega}$ group delay [sec/m]

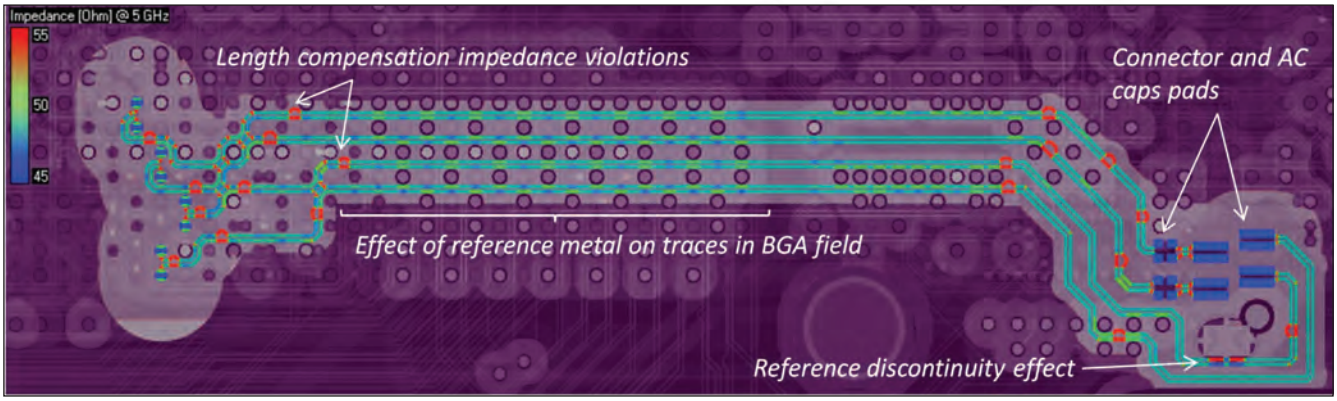

Fig. 8 Example of how the reference conductors can change the impedance of traces on a design with traces going through BGA breakouts.

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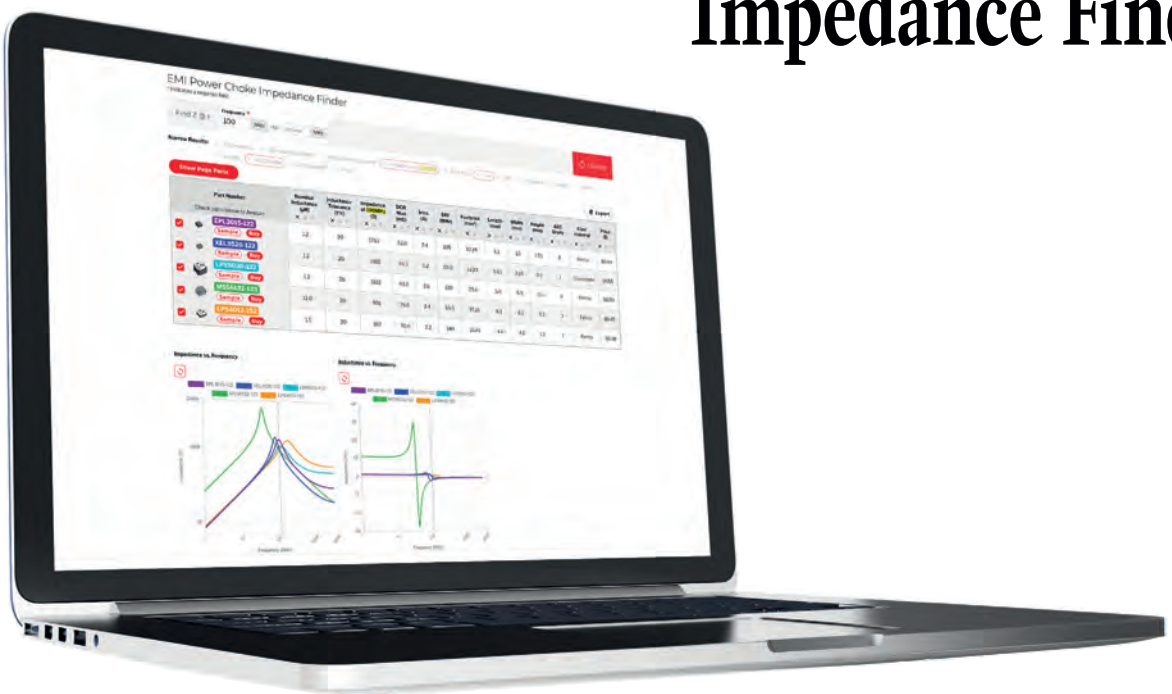

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Ultra-Fine Line Differential Pair Design with No Return Plane

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Conventional differential pairs in circuit boards have adjacent return planes which strongly affect their differential impedance. Due to constraints in keeping the total board thickness under a maximum value and using linewidths larger than 4 mils, the coupling between the two lines in a differential pair is usually much less than the coupling of each line to the adjacent plane.

With the recent introduction of the Averatek Semi-Additive Process (A-SAP™), linewidths under 1 mil are possible using the same fabrication processing equipment as for traditional 4 mil wide lines. This opens up a new design space where the coupling between the traces can be much larger than the coupling to the adjacent plane. This means a new set of design rules must be applied for ultra-fine line differential pairs. This article is part 3 in the Ultra-Fine Line Design Guide series.

Methodology to Explore Fine Line Geometries

In a previous paper, a methodology was introduced to explore the design space of a differential pair to find the optimized features and achieve a target impedance with other parameters as a constraint. In addition, we introduced the span of a differential pair as a new metric to describe the extent of its boundaries. The geometrical features of a differential pair are defined in ***Figure 1***.

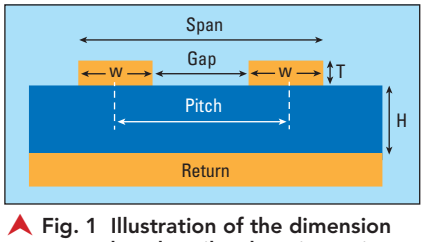


Fig. 1 Illustration of the dimension terms used to describe the microstrip differential pair.

In this article, we use this methodology to explore the design space for a differential pair when the return plane is far enough away that coupling to it is negligible. This is a possible option only for very fine line traces with a small span, which is the realm of ultra-fine line widths.

When Does the Coupling to the Adjacent Plane Not Matter?

The ultra-fine line capability of the A-SAP™ process enables an interesting configuration for differential pairs with much higher coupling between the traces than to an adjacent plane. This is the configuration in a CAT5 twisted pair cable, for example.

As the coupling between two traces increases, there is a point at which the coupling to an adjacent plane reduces to an insignificant level. One way to picture this is to consider the return current distribution in the adjacent return plane for a differential signal.

When the two traces are separated by their line width, and the return plane is located a distance away to result in 100 Ohm differential impedance, the return currents in the plane of each line in the differential pair is well localized under each trace, separate and succinct. It is not true that the return current of one line is carried by the other. The return current for each line is carried in the plane, spatially separated; this is shown in ***Figure 2a***.

However, when the plane is moved farther

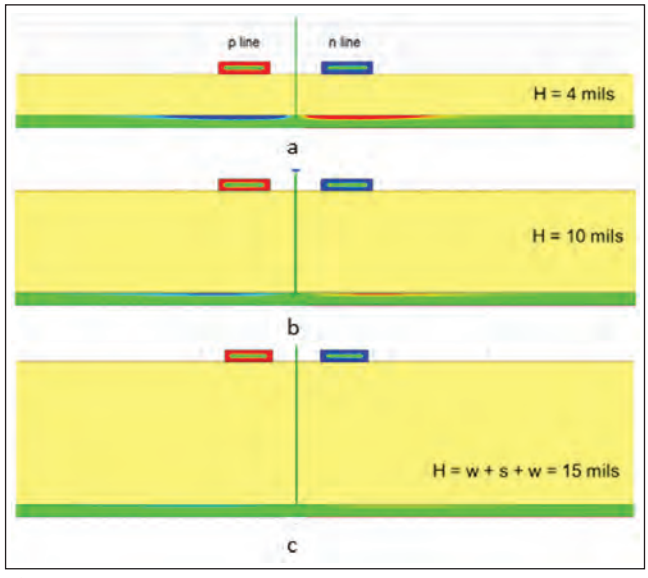


Fig. 2 The current distribution in the return plane for a differential signal in 2 cases: a) height = 4 mils, b) height = 10 mils, c) height = 15 mils, simulated in Ansys Q2D.

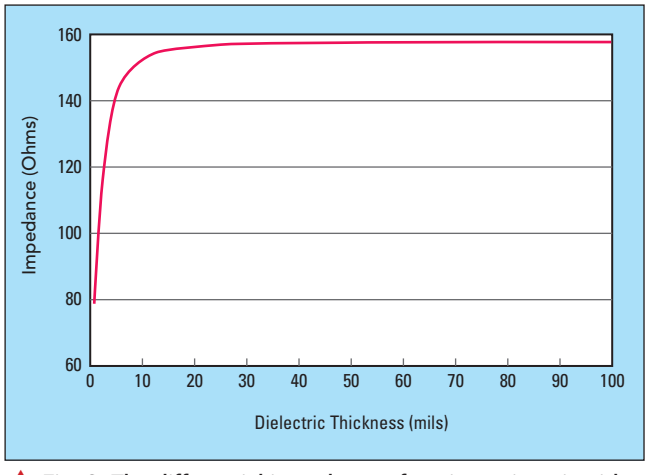


Fig. 3 The differential impedance of a microstrip pair with fixed 2 mil line widths and 6 mils gap separation as the return plane is moved farther away.

away, the differential impedance increases, and the return currents for a differential signal begin to overlap and cancel out. When the plane is as far away as twice the gap separation, some of the return currents from the two lines have canceled out and the return current distribution in the plane is reduced as shown in ***Figure 2b***.

When the return plane is so far away that all the return currents of the two lines completely overlap in the plane, there is no return current in the plane and the plane can be removed with no impact on the differential impedance. This is shown in the ***Figure 2c***, where the height is 15 mils. In this case, it is true that the return current of one line is carried by the other. And, in this situation, the plane has no impact on the differential impedance of the pair.

Using the methodology developed previously, we can explore this design space to evaluate how far away the plane needs to be so that it has no impact on the differential impedance of the pair. In this case, the differential impedance is only about the coupling between the two lines in the pair.

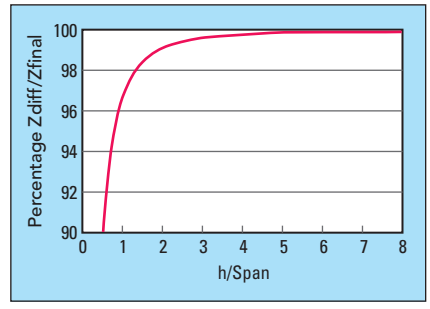


Fig. 4 Relative impact on the differential impedance, compared to the limiting impedance, from the dielectric spacing, h, normalized to the span.

In this analysis, the line width and the space between the two traces were fixed and the differential impedance was calculated using the 2D field solver in Keysight's ADS as the trace height above the return plane, h, was increased. ***Figure 3*** is a plot of the differential impedance vs. dielectric thickness (h) for a 1 oz trace thickness where the trace width was fixed at 2 mils and the gap separation was 6 mils. This would be an uncoupled differential pair if the plane was very close.

This analysis shows that when the dielectric thickness is very large, the differential impedance is completely independent of the distance to the plane (h). The limiting impedance is only about the conductor thickness, the line width, and the gap separation between the two lines. This is the case when the plane is so far away that the coupling between the two lines is much larger than the coupling to the plane below.

Using this limiting value of the differential impedance when the plane is very far away allows one to plot the relative impact on the impedance from the distance to the bottom plane, h. The results showing the differential impedance for a span of 10 mils, with 1 oz copper traces as the dielectric thickness, h, increases, are shown in ***Figure 4***.

To achieve 97% of the final differential impedance, the plane needs to be at least one span away. This analysis was repeated for spans of 4, 10, and 50 mils. For each span, the limiting impedance was calculated and used to normalize the differential impedance. Likewise, the span for each case was used to normalize the dielectric thickness. This analysis is shown in ***Figure 5***.

Surprisingly, a dielectric height to the adjacent plane equal to the span of the differential pair is a good metric for how far away the plane needs to be to have all the return currents overlapping and the plane play no role at all. The span is a rough measure of the extent of the fringe field lines from the two lines in the pair.

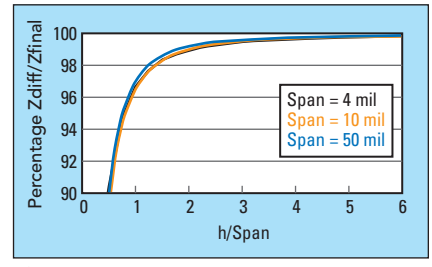


Fig. 5 Relative impact on the differential impedance, compared to the limiting impedance, for the dielectric height, h, normalized to the span for the case of three different spans. Each trace was 1 oz copper in this simulation.

This is the origin of a powerful rule of thumb: in order to have a differential pair so tightly coupled that an adjacent plane does not affect its differential impedance, the plane should be

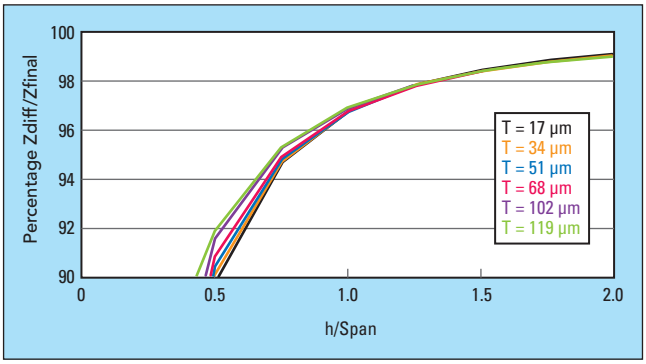


Fig. 6 Relative differential impedance as the dielectric thickness is changed. Independent of the conductor thickness, the differential impedance is within 97% of the final value when the dielectric thickness is equal to or greater than the span, even using extreme conductor thicknesses.

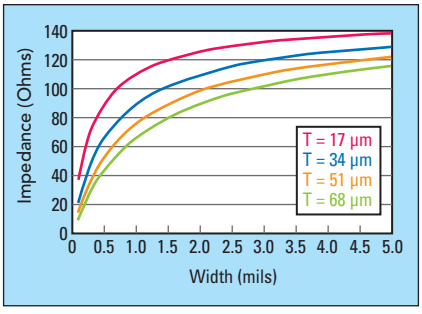


Fig. 7 The differential impedance of a pair with line width = gap separation, and the return plane very far away, for different conductor thicknesses.

farther away than the span of the pair.

This rule of thumb is an important guideline to identify when a differential pair's impedance is independent of any return plane. For example, if the span of a differential pair is 5 mils, then a return plane more than 5 mils below the traces will have no impact on its differential impedance. In this case, the differential impedance of the pair is only related to their conductor thickness, line width, and spacing.

This rule of thumb also applies to thin and thick conductors. ***Figure 6*** shows the same analysis for the relative differential impedance for a span of 4 mils, line width of 1 mil for each trace, and fixed gap separation of 2 mils, using conductor thicknesses of 0.5 to 3.5 oz copper traces. In this extreme environment, the differential impedance has achieved its nearly final value with a dielectric thickness of about 1 span for all conductor thicknesses.

This rule of thumb is surprisingly robust. It applies to 1 mil wide traces and ½ oz thickness, or an aspect ratio of trace thickness to line width of about 0.5, all the way to extreme aspect ratios of almost 5.

A New Behavior Emerges in the Ultra-Fine Line Regime

This rule of thumb identifies when the design constraints eliminate the impact of the return plane on the differential impedance.

In this special case, when the return plane is moved so far away that there is no coupling to it, the differential impedance of the pair is determined only by the line-to-line coupling. ***Figure 7*** shows that as the line width decreases, keeping the gap separation equal to the line width, the differential impedance decreases as well.

Figure 7 shows that for a conductor thickness of even 2 oz copper or 68 micron, and line widths wider than 5 mils; the regime of conventional circuit board technology, the differential impedance, determined only from the line-to-line coupling, is much greater than 100 Ohms. To achieve a target impedance of 100 Ohms, in conventional technology, coupling to the adjacent plane is required to bring the differential impedance down to 100 Ohms. Having an adjacent plane is a critical feature to achieve 100 Ohms in conventional board technology. Otherwise, the differential impedance will always be larger than 100 Ohms.

Figure 7 also shows that as the linewidth decreases, the differential impedance continues to drop. The coupling between the traces from their adjacent side walls transitions from a second or third order effect to a first order effect. In this special case of line width equaling gap separation, the trace thickness to the line width is about 1, and the differential impedance is about 100 Ohms, without an adjacent return plane.

This is an important observation for high aspect ratio, ultra-fine lines. The additional fringe field coupling between the taller side walls can provide enough coupling to bring the differential impedance of a pair closer to 100 Ohms. In the special case of traces with an aspect ratio of 1, with the line width equaling the gap separation equaling the conductor thickness—when the plane is very far away, and the differential pair is sitting on a relatively thick dielectric slab—the differential impedance is coincidently about 100 Ohms. This behavior is shown in the simulation in ***Figure 8***.

This is a remarkable observation and is the origin of another simple rule of thumb: for traces with an aspect ratio of 1, and a trace width equaling gap separation, the differential impedance of a pair is 100 Ohms when the return plane is very far away, and the pair is effectively sitting on a dielectric slab with a dielectric constant of 4.

It is a convenient coincidence that this aspect ratio of 1 for conductor thickness and gap separation contributes just the right amount of fringe fields to bring the differential impedance to 100 Ohms without the need for an adjacent return plane. This is an easy rule of thumb to remember and offers a simple anchor point from which to scale other conditions.

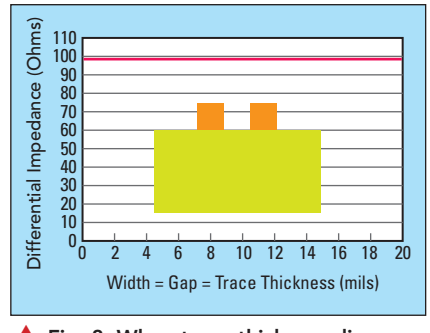
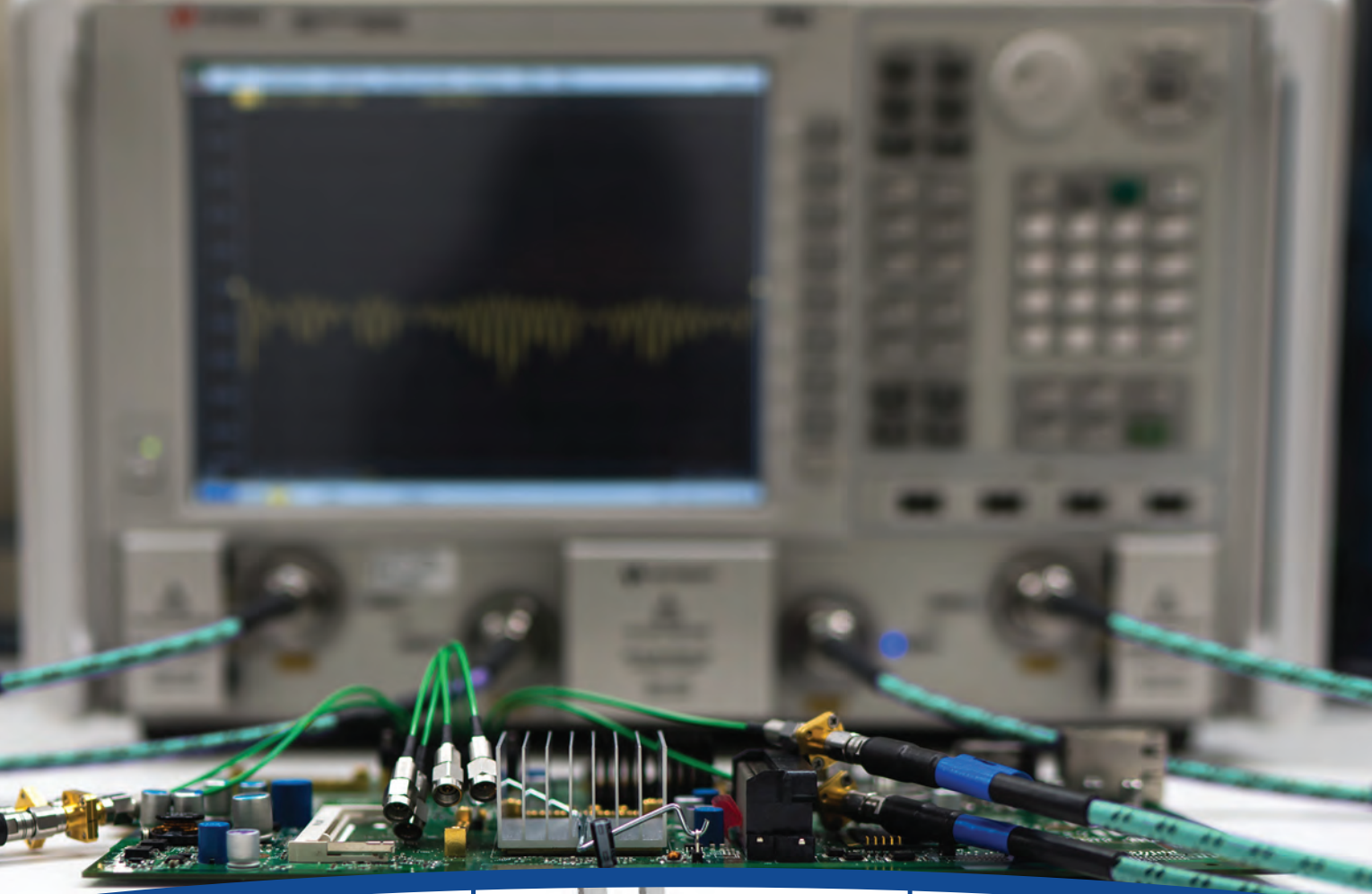
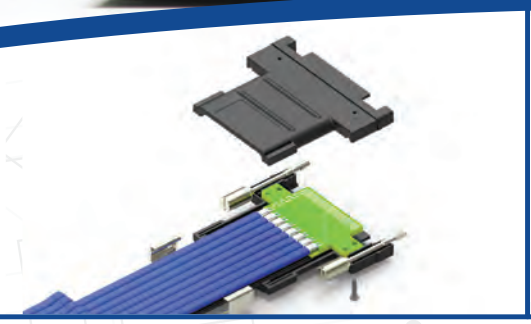
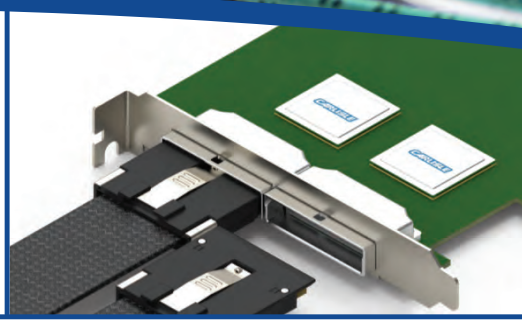


Fig. 8 When trace thickness, line width and gap are the same value, and the plane is very far away, the differential impedance is close to 100 Ohms. Because the fringe fields between the two traces are invariant with the ratio of the dimensions, keeping the ratios fixed means the differential impedance is fixed over all dimensions.

For example, for a thinner conductor, the differential impedance will go up. For a larger gap separation, the differential impedance will go up. For a narrower line width, the differential impedance will go up. For an aspect ratio greater than 1, the gap separation would have







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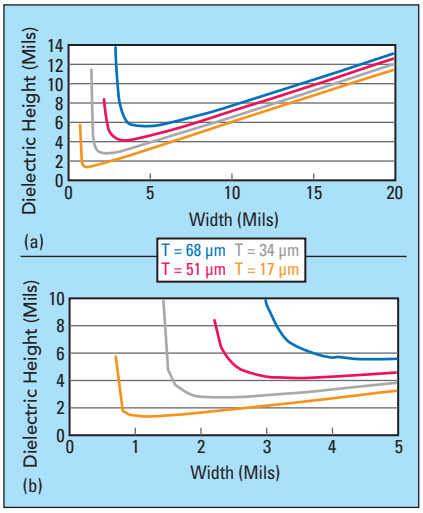

Fig. 9 Example of the design space for a 100 Ohm differential pair with a line width = gap separation. As the line width decreases, the dielectric height to the adjacent return plane must decrease to maintain the 100 Ohm impedance. Over a range of line widths to 20 mils (a); zooming in to the range of line widths of up to only 5 mils (b).

to increase to maintain 100 Ohm differential impedance.

This rule of thumb applies to any pair with any linewidth having an aspect ratio of 1. However, since conductor thicknesses in conventional circuit boards are on the order of 0.2 to 3 mils, this rule of thumb really applies specifically to ultra-fine line geometries, with line widths less than 3 mils.

When the aspect ratio is less than 1, the differential impedance is higher than 100 Ohms for the special case of the line width equaling gap separation. To achieve a 100 Ohm target impedance, the return plane must be moved closer to the pair to increase the coupling of the two lines. This defines the design space for 100 Ohm differential pairs, and is shown in ***Figure 9***.

This map of design space for a 100 Ohm differential pair clearly shows the new emergent behavior starting when the aspect ratio is greater than about 0.5 and the edge-to-edge fringe field coupling becomes a first order effect. This is the regime of ultra-fine line geometries.

There are two important consequences from this behavior. First, it is possible to achieve a 100 Ohm target impedance when the return plane is moved farther away than the span of the differential pair. This means that when ultra-fine line technology is mixed on the same layer as conventional line width technology, the 100 Ohm differential impedance can easily be matched using appropriate line width and gap separation.

The second consequence is that for an aspect ratio of conductor thickness to line width larger than 1, the gap separation will generally have to be larger than the line width to hit a 100 Ohm target impedance. Higher aspect ratio geometries will require a ratio of less than one line width to the gap separation.

The regime of ultra-fine lines, with aspect ratios of trace thickness to line widths greater than 0.5, requires a re-calibration of our design intuition to include the first order effect of the edge-to-edge coupling, without the need for an adjacent return plane. These are important considerations when mixing ultra-fine line and conventional circuit board technologies.

For example, for 1 oz copper traces, when the line width is 5 mils and the gap separation is 5 mils, the dielectric height to the adjacent plane would have to be 4 mils to achieve a target impedance of 100 Ohms. Any other pairs sharing this layer with a span of less than 4 mils would have a differential impedance independent of the adjacent plane. This is a new design regime which specially applies to ultra-fine line geometries.

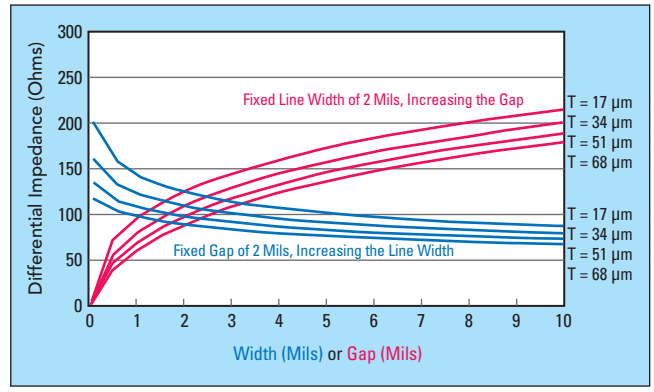

Fig. 10 Differential impedance of a microstrip pair with return plane far away, keeping either the line width or gap separation fixed.

Design Space for Ultra-Fine Lines with No Return Plane

When mixing conventional and ultra-fine line geometries on the same layer, the ultra-fine line differential pairs routed with their smallest span will generally not couple to the adjacent plane. Our design intuition in this regime is very different than when the adjacent plane influences the differential impedance.

In the special case of differential pairs with their dielectric thickness to the return plane farther away than their span, their differential impedance is only about their line width, gap separation, and conductor thickness. As we would expect, the differential impedance is more sensitive to the gap separation than the line width.

Of course, for a fixed gap separation, as the line width increases the differential impedance will decrease, but it is only slowly varying with line width. The faraway edges of each line do not couple as strongly as the adjacent edges of the two traces that make up the differential pair.

However, the differential impedance is strongly dependent on the gap separation, as this is the region where most of the coupling between the two traces occurs. This means that for a fixed line width, the differential impedance will change rapidly with the gap, but not so rapidly with line width.

In each case, the differential impedance will decrease for thicker conductor due to the additional fringe field coupling from the relatively larger side walls.

These two general trends, with a return plane very far away, are shown in ***Figure 10*** for up to a 10 mil span dimension. In one case, the line width is fixed at 2 mil and the gap separation is increased, and in the other case the gap separation is fixed at 2 mils and the line width of each line is increased. In all cases, the dielectric thickness is adjusted so that it is always larger than 3× the span, effectively infinitely far away.

This analysis shows that in this regime where the return plane plays no role, the gap separation has a

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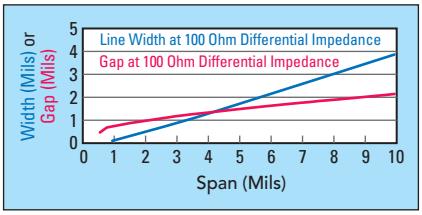

Fig. 11 Design space for 100 Ohm differential impedance as the span changes for 1 oz copper traces and the return plane is very far away. When sweeping line width, the gap was 2 mils. When sweeping the gap, the line width was 2 mils. There is one unique combination of line width and gap separation that results in 100 Ohm differential impedance.

stronger impact on the differential impedance than the line width.

We can use the Johnny Cash Principle, introduced in part 2, to define design space for a 100 Ohm differential pair as its span changes. At each value of the span, there is one unique value of line width and gap separation that results in 100 Ohm differential impedance.

This 100 Ohm design space is shown in ***Figure 11***, using the special case of 1 oz copper traces, all with the coupling between the two lines much larger than the coupling to any distant plane.

For example, in the case of 1 oz copper for a 100 Ohm target impedance when the span is on the order of 4 mils, the gap will be about 1.3 mils and the line width will be about 1.3 mils.

Mixing Conventional and Ultra-Fine Line Technology

One strategy for mixing conventional and ultra-fine line traces on the same layer is to use as wide a trace as is practical for its lower conductor loss, and only use the ultra-fine lines where the higher interconnect density is needed for routing in congested breakout regions.

If the top layer microstrip traces are designed with ¼ oz copper and a 5 mil wide line and 5 mil space differential pairs, a 100 Ohm differential impedance will be achieved with about a 4 mil thick dielectric to the adjacent plane. Any pair with a span smaller than 4 mils will not be influenced by the adjacent plane.

On this same layer, if ultra-fine lines were used, with a conductor thickness of 6 micron (¼ oz copper), line widths of 6 micron, and a gap of 6 micron, their differential impedance would be 100 Ohms. These dimensions would enable four routing tracks between 0.5 mm BGA pads. These high-density tracks could be used to fan out from the BGA escape to a coarser routing field. ***Figure 12*** illustrates two different transitions from the ultra-fine line to the coarser traces while maintaining 100 Ohms differential impedance.

If the transition region is short, even if the differential impedance is not held constant, the impact from this discontinuity may be acceptable. This mixed line width approach optimizes the interconnect density where needed and the lower loss from wider traces where it is available, while maintaining a constant 100 Ohm differential impedance.

Conclusion

With the recent introduction of ultra-fine line fabrication technologies, it is possible to mix very fine line traces with conventional circuit board traces on the same layer. This provides the advantage of using ultra-fine lines for regions of congested routing while wider traces can be used for longer paths where reducing signal loss is important.

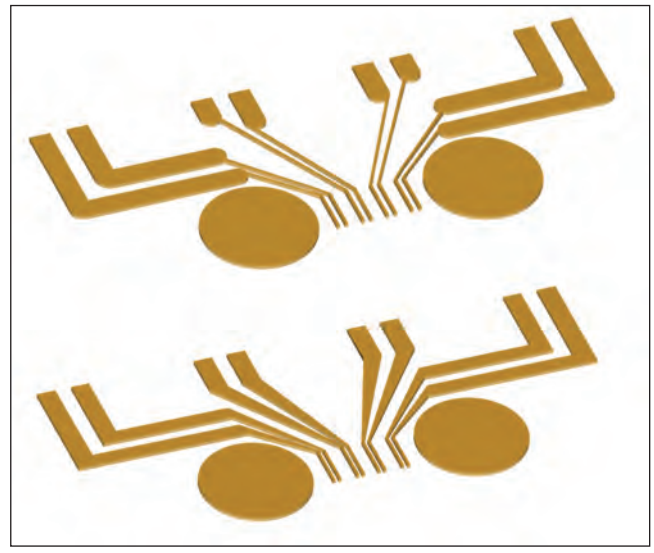

Fig. 12 Using 6 micron line width, trace thickness, and gap, results in 100 Ohm differential impedance with four routing traces between 0.5 mm pitch BGA pads. Top: keeping the aspect ratios nearly fixed. Bottom: Adjusting the width as the gap increased to maintain 100 Ohm differential impedance.

However, when these very different trace widths are routed on the same layers, and the differential impedance of pairs are kept at 100 Ohms, new design guidelines emerge for the ultra-fine line traces due to two important emergent behaviors.

First, when their span is less than the dielectric height to the adjacent plane, the plane has no influence on the differential impedance. It is about the line width, gap separation, and conductor thickness; there is one unique combination of line width and gap separation for a specific span. This defines the design space for these traces.

The second important design consideration is that in this regime of very fine lines, the aspect ratio of conductor thickness to trace width increases over conventional technology, and the side wall coupling between the two traces becomes a first order effect. This new coupling must be taken into account when designing the differential pair.

In the extreme case, with no adjacent return plane, a differential pair with trace thickness, line width, and gap separation all of the same order will result in a 100 Ohm differential impedance.■

REFERENCES

1. E. Bogatin, "New Electroless Process Promises Finer PCB Features," *Signal Integrity Journal*, 2021, Web: https://www.signalintegrityjournal.com/blogs/4-eric-bogatin-signal-integrity-journal-technical-editor/post/2122-new-electroless-process-promises-finer-pcb-features.
2. E. Bogatin, C. Suresh, M. Piket-May, H. Basit, and P. Dennig, "Utilizing Fine Line PCBs with High Density BGAs," *Signal Integrity Journal*, 2022, Web: https://www.signalintegrityjournal.com/articles/2386-utilizing-fine-line-pcbs-with-high-density-bgas.
3. E. Bogatin, C. Suresh, M. Piket-May, H. Basit, and P. Dennig, "Exploring Design Space for Fine Line Differential Pair Transmission Lines," *Signal Integrity Journal*, 2022.

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Understanding Via Impedance

Donald Telian
SI Guys, Oakhurst, Calif.

If you routinely give attention to trace impedance but are not accustomed to thinking about via impedance, this article is for you. Or, if you are paying attention to via impedance yet are unsure what dimensions will yield the right impedance, this will help with that too. So, when should I use an 8 mil drill?

Why Should I Care?

Serial links can fail because of impedance mismatches, or discontinuities. In practice, discontinuities are causing more problems than loss. While loss degrades a signal somewhat predictably and can be compensated by equalization, discontinuities cause reflections that are much harder to tame. So, fix the discontinuities and you fix the signal. An example of a 400% eye improvement achieved by correcting via impedance is shown in the article, "Moving Higher Data Rate Serial Links into Production – Issues & Solutions;" a mere 1% of the interconnect.[1] Another method to improve via impedance is shown in "New SI Techniques for Large System Performance Tuning," and its resulting performance improvement measured in hardware.[2]

Although they are small, vias can significantly impact performance. This first became apparent when ¼ wavelength stubs crept into systems. A via stub left in a ¼ in. thick backplane can completely remove a 12 Gbps signal, per the approximation 3/12 (yes, just use 3 divided by Gbps and get inches).[3] While stubs can be disastrous, via impedance mismatch is also increasingly problematic as data rates increase. But how can we better understand the impedance of vias?

Enter Via Modeling

A few decades ago, while my RF friends were busy with exotic 3D solutions of vias, we would place a 0.5 pF capacitor in our interconnect model at via locations and call it good. Over time, we learned that modeling vias as a transmission line is a better approach. Some tools implement fast via solvers[4] that expand on the transmission line concept to deliver correlated accuracy, as described "Fast, efficient, and accurate: via models that correlate to 20 GHz."[5] Yet even if you don't have access to a fast via solver, it is possible to gain an intuitive sense of via impedance, as described here. And if you want to try out a via solver, a link is provided at the end of this article.

Building Impedance Intuition

To build our intuition on what via dimensions will yield impedances we want, let's begin with the more familiar differential trace shown in ***Figure 1***. Indeed, vias behave a bit like traces—albeit in the Z dimension. Figure 1 shows stripline trace impedance versus width, spacing, and distance to ground planes (X-axis represents W=S=H1=H2 per the cross-section view). Interestingly, all dimensions yield impedances close to what we typically want, and minor adjustments are used to dial in the value more precisely. For example, increasing either or both H values moves the reference plane further away, making the trace more inductive, thus raising the impedance (Z=sqrt[L/C]). Widening the trace (W) makes the trace more capacitive, thus lowering its impedance. Visualize how these two changes impact impedance, because we are about to apply them to via structures.

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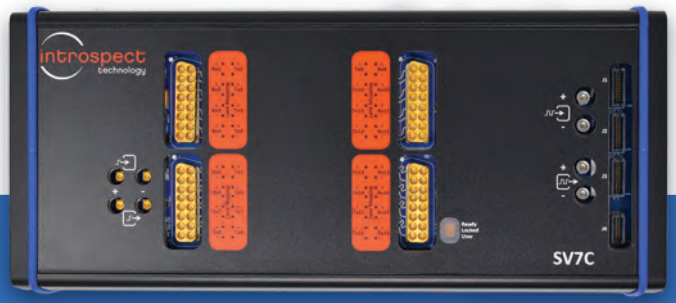

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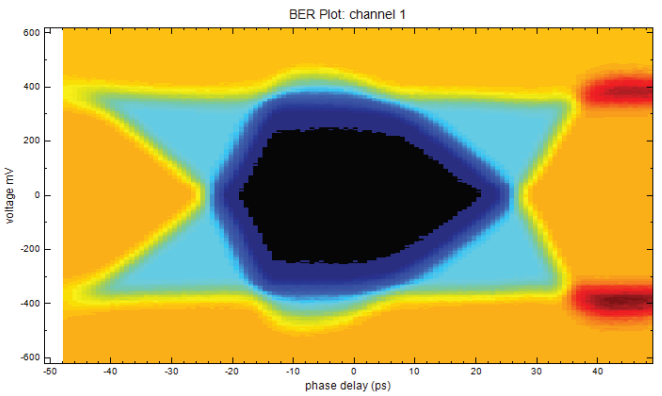

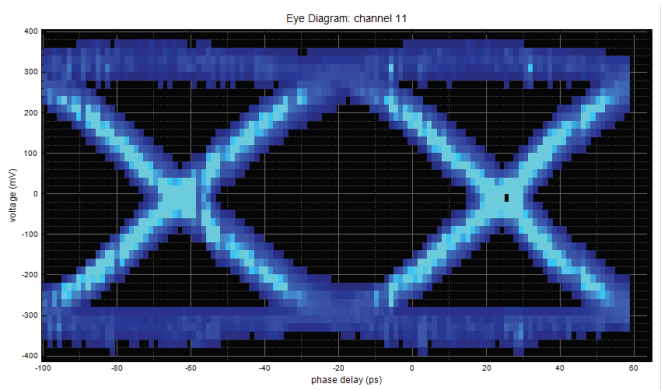

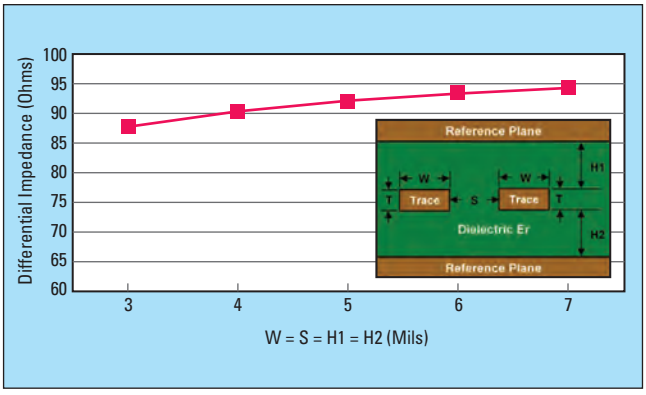

Fig. 1 Differential trace impedances.

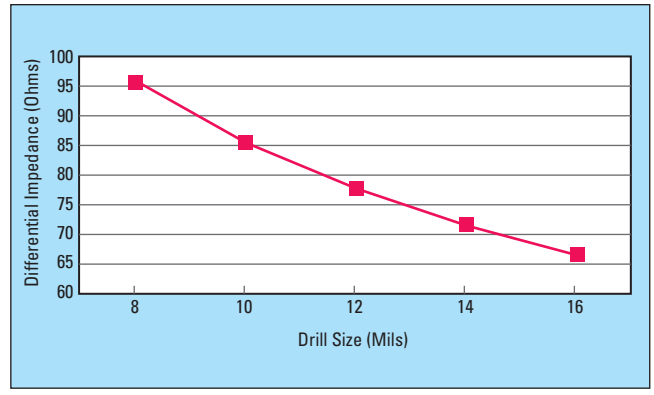

Fig. 2 Differential via impedances.

Figure 2 plots differential via impedance versus common drill sizes on the X-axis. Pad sizes are drill+10 mils and circular antipad sizes are drill+20 mils. Spacing is 1 mm as would be found under a BGA or near a connector. The first thing we notice is the range of impedances has increased more than 4× when compared to the range of trace impedances in Figure 1. This wider range makes via impedance more challenging to control. Like traces, we can make changes to a via's structure to adjust its impedance. For example, widening the antipads—or connecting them into an oval "racetrack" shape—moves the reference plane further away (like increasing trace H in Figure 1) making the via barrel more inductive thus raising its impedance. In contrast, increasing the drill size widens the barrel (like increasing trace W) making it more capacitive, hence lowering its impedance.

Again, the challenge with vias is the 4×+ impedance range compared to the narrower range associated with traces—seen clearly by comparing Figure 1 and Figure 2. As structural adjustments for traces and vias have similar dimensions, they also have similar effects on impedance—perhaps 5Ω or 10Ω in either direction. As such it becomes difficult to get 16 or even 12 mil vias close to 100Ω because their "natural" (i.e., no structural modifications) impedances are ~70Ω. Thus, it should become apparent why 8 mil drills are gaining in popularity in a world somewhat reluctant to move towards 85Ω impedance—which is the "natural" impedance of the more common 10 mil via.

Digging Deeper

You might be objecting to my generalizations because I did not state my dielectric constant (Dk). You're right—it is 3.3. Dk proportionally raises capacitance and hence inversely affects impedance. As such, the first time I solved 10 mil vias with a Dk = 3.0, I found them closer to 100Ω than expected. With common Dk values varying 50% (3.0 to 4.5), Dk is indeed an important consideration. So, when using the differential impedances shown in Figure 2, if your Dk is higher than 3.3, your impedance values will be lower. Likewise, if your Dk is lower than 3.3, your impedances will be higher. For example, as Dk ranges from 3.0 to 3.6, the Figure 2 impedances change ± ~4Ω.

We should also discuss differential trace and via spacing. As traces or vias get closer together they become more capacitive and hence impedance decreases. While the trace impedances shown in Figure 1 can be increased ~10Ω by separating the traces, via impedances will decrease from those shown in Figure 2 as vias move closer together. However, due to their associated pads, via barrels cannot move closer together than ~20 mils, making it difficult to decrease impedance by more than ~5Ω.

Also, be advised that as we pass 28 Gbps NRZ data rate, we need to stop thinking of vias as a single impedance, but instead as a structure whose impedance dips at the pads and rises in the barrel. At this data rate those elements are within the relevant feature size and, therefore, are modeled separately.[6]

Conclusion

As you start down the road of grappling with via impedances—and more tools and measurements become available for the same—the task will simplify, just as it did for traces. My goal has been to give you a reference point to make the task of implementing via impedances—thus removing via impedance discontinuities—less daunting. Want to try out automated solvers with your via dimensions? Download a free trial of Signal Integrity Toolbox which includes a Via Editor tool.[7]

*This article is an excerpt from Donald Telian's new book "Signal Integrity, In Practice." A Practical Handbook for Hardware, SI, FPGA, and Layout Engineers. Available at Amazon.■

REFERENCES

1. D. Telian, S. Camerlo, K. Matta, et al. ,"Moving Higher Data Rate Serial Links into Production – Issues & Solutions," *DesignCon, 2014*, page 4.
2. D. Telian, M. Steinberger, B. Katz, "New SI Techniques for Large System Performance Tuning," *DesignCon, 2016*, page 21.
3. D. Telian, "Adapting Signal Integrity Tools and Techniques for 6 Gbps and Beyond," SiGuys, *CDNLive!, slides 1-33,* 2007, slide 5.
4. D. Telian, S. Camerlo, M. Steinberger, et al., "Simulating Large Systems with Thousands of Serial Links," *DesignCon, 2012*, page 4.
5. M. Steinberger, D. Telian, E. Brock, "Fast, Efficient and Accurate: via Models that Correlate to 20 GHz," *DesignCon, 2013*.
6. D. Telian, "Which Discontinuities are Small Enough to Ignore?" *Signal Integrity Journal RSS, April 2022*, Figure 2.
7. Signal Integrity Toolbox Free Trial, www.mathworks.com/products/signal-integrity.html.

Donald Telian *is a Signal Integrity Consultant, the owner of SiGuys, and the author of the book "Signal Integrity, In Practice" now available at Amazon. He has worked in Signal Integrity for 40 years.*

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The Case for Split Ground Planes

Eric Bogatin, Technical Editor
Signal Integrity Journal

The risk of causing signal integrity, power integrity, and EMI problems with a split in the ground plane strongly outweighs the potential benefit; there is only one case when there might be a benefit for a split ground plane. It is explained here.

Once connectivity is established, the only thing an interconnect is going to do is add noise. When an engineer designs interconnects, they must design them to reduce the noise they might generate. When making design choices, we are always asking the question, what is the noise problem we are trying to fix, and how do we engineer the interconnects to reduce this source of noise? If you are considering using a split ground plane, one must first answer the question, what is the problem a split ground plane is trying to fix? And what are the potential other problems that might be created, the law of unintended consequences?

Why Continuous Return Path Planes

The first step in engineering interconnects to reduce noise is to provide a continuous, low impedance return path to control the impedance, which controls reflection noise, and reduces the crosstalk between signals that share the same return conductor.

A wide, continuous ground plane adjacent to a signal trace will be the lowest crosstalk configuration. Anything other than a wide plane means more crosstalk between signal paths sharing this return conductor. This means never add a split or gap in the return path. That would run the risk of a signal trace inadvertently crossing this discontinuity.

If a signal crosses over a split ground plane, there are two effects that compound each other. Crossing a split creates a higher impedance path for return currents that must cross the split and forces return currents from multiple signals to overlap through the same higher impedance common path.

This creates the trifecta of problems: reflections from the return path discontinuity, ground bounce from the higher inductance return path, and EMI from the difference in potential between the two regions of the planes in which the return currents flow.

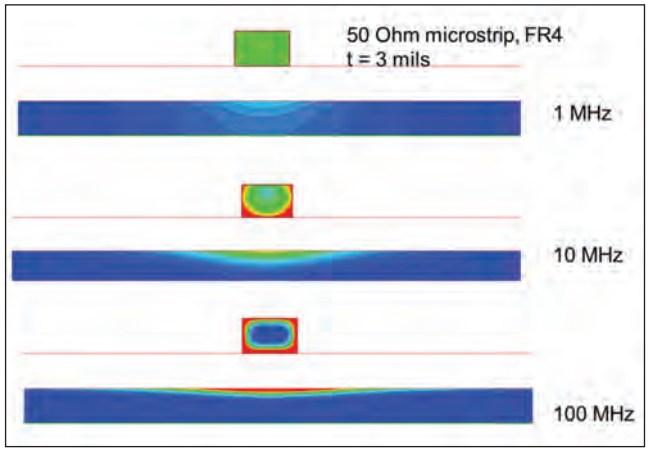

Fig. 1 Current distribution in the signal and return conductors at three different frequencies. The current redistribution at higher frequency is driven by the currents taking filament paths with the lowest loop inductance.

Therefore it is never a good idea to add a split in the ground return plane; you take a big risk of signals routed crossing this split.

However, there is one potential problem a split ground plane solves, provided the split or gap in the return plane is always parallel to the signal path, and return currents do not cross this gap. It is the minor issue of crosstalk from resistive coupling.

Where Return Currents Flow

The path return currents take in a ground plane depends on the routing of the signal paths. The signal and return paths cannot be considered separately; they are linked together. The path the currents take in a signal and return conductor are dictated by the path of lowest loop impedance. If there were a path the signal-return current took that was lower impedance, there would be a lower voltage drop along that path and currents would flow from the higher voltage paths to the lower voltage paths until all conductors, normal to the direction of propagation, were at an equipotential. This means that of the multiple paths signal-return currents could take, the currents will flow in the path to minimize the loop impedance of all possible paths.

Usually, the signal trace is narrow and confines the signal current to a very specific path. The return current can flow in the adjacent ground plane anywhere, unconstrained except for the plane edges. It will take the path so that the loop impedance of the signal-return path is minimized. To first order, the impedance of the signal-return path is frequency dependent and related to:

$Z = R + j\omega L$

In this equation, Z is the loop impedance of the current loop path, R is the series resistance of the loop, and L is the loop inductance of the path.

Imagine the signal-return path currents as composed of continuous current filaments taking any path they can down the interconnect. The filaments that have the most current are those with the lowest loop impedance. The more current flowing down one of these filaments, the higher the voltage drop across this series impedance. This pushes more current into adjacent higher impedance filaments until the cross section of current distribution, balanced by the impedance of each filament and the amount of current in each filament, create an equipotential across the direction of propagation.

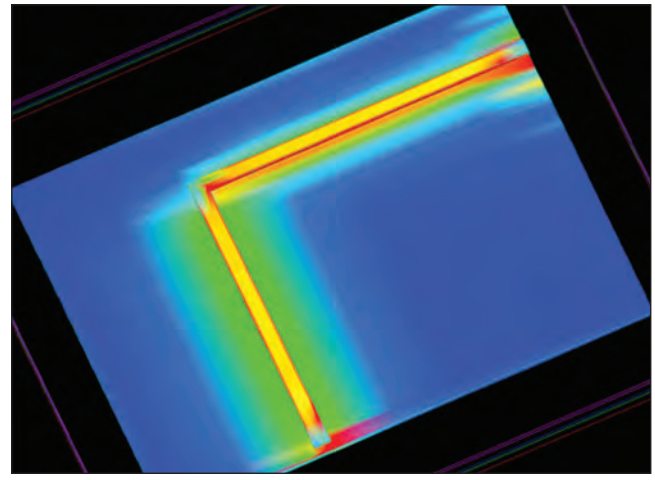

Fig. 2 Current flow in the return path at 1 MHz, when the signal path changes.

There will always be a frequency, above which the ωL term dominates, and the current paths are driven by the path of lowest loop inductance. This is the region we refer to as the skin depth region. The current redistribution for lowest loop inductance is what drives the skin depth effect.

The lowest impedance path is when currents within the same conductor are farthest apart, to reduce the partial self-inductances, but are closest together between the signal and return paths, to increase the partial mutual inductances. This is illustrated in ***Figure 1***, showing the current distributions in a simple microstrip at 1, 10, and 100 MHz; simulated with Ansys Q2D.

This means that in the high frequency regime, the return currents are always flowing directly underneath the signal currents. The path underneath the signal currents is always the lowest loop inductance path. Any current filaments away from this path will have a higher impedance, a higher voltage drop, and flow to the lower voltage filaments, directly under the signal.

As the signal conductor meanders over the surface of the ground plane, the return currents will follow right along under the signal path. ***Figure 2*** shows an example of the return current distribution in a plane when the signal conductor changes direction, simulated for 1 MHz frequency components.

Return Current at Low Frequency

At low frequency, when the loop impedance is dominated by the R term, the current distribution in the return plane is not driven by the loop impedance; it is driven by the loop resistance. In the signal path, the current will spread out uniformly as any filament path in the signal conductor will have roughly the same resistance.

But the current filaments in the return path with the lowest R will be those that are shortest. This means that return currents will take the shortest paths, independent of the signal paths. As frequency increases,

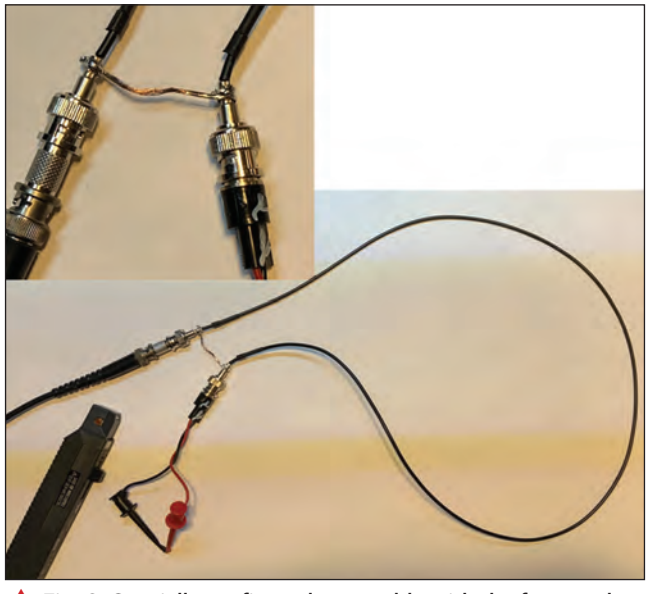

Fig. 3 Specially configured coax cable with the front and back of the shield shorted together.

the return current will redistribute to transition from the path of lowest R to the path of lowest L.

This was demonstrated in a simple experiment. A coax cable was shorted at the far end so that a DC current loop, driven by a function generator, would flow from the signal conductor and back through the return. At the front of the coax, the shield, which carries the return current, was shorted between the front of the coax and the back end of the coax as shown in ***Figure 3***.

At DC, the return current will flow through the shunt between the front and back of the shield, which is a lower resistance path, instead of flowing all the way down the shield to the far end where the signal and return currents are shorted together.

To measure the current that flows through this path, a Hall effect current clamp was placed around this shunt path. This measures the current flowing through this specific path. The function generator was used to drive a constant 60 mA amplitude sine wave current through the coax cable and the frequency swept from 1 kHz to 10 MHz. The currents were measured with the Hall effect current probe and a Teledyne LeCroy WavePro HD 12-bit, 8 GHz bandwidth scope.

At low frequency, all the return current flowed through the shunt path. But, as frequency increased, less current flowed through the shunt and more current flowed along the higher resistance but lower loop inductance path of the coax shield, with the return current in close proximity to the signal current. ***Figure 4*** shows the measured current amplitude in the signal-return loop at the far end, flat with frequency, and the measured current amplitude in the shunt, which drops off with a 1-pole response, above about 10 kHz.

This illustrates that above about 10 kHz, all the return current will always flow in the path directly adjacent to the signal current to reduce the loop inductance of the signal-return path. But, equally important, the return currents below about 10 kHz will always flow in the path for lowest resistance.

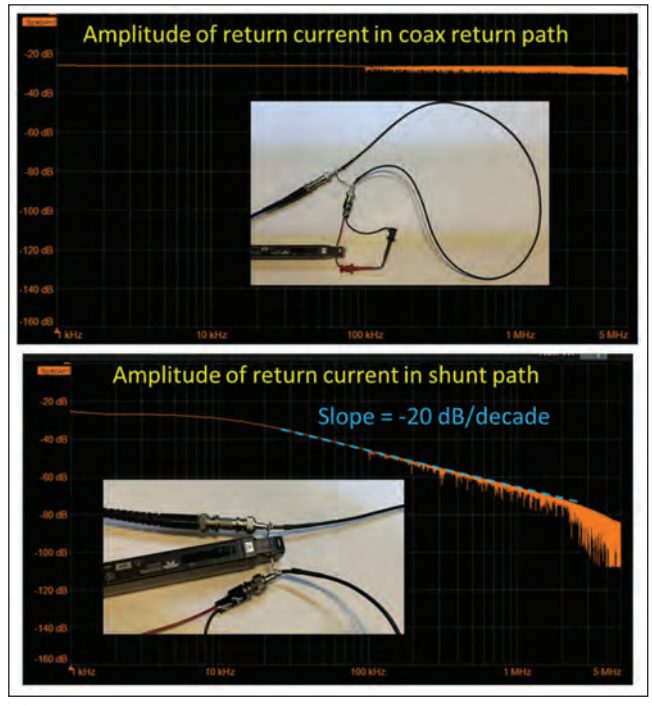

Fig. 4 Measured return current in the shunt path dropping off above 10 kHz, measured with a Teledyne LeCroy WavePro HD scope.

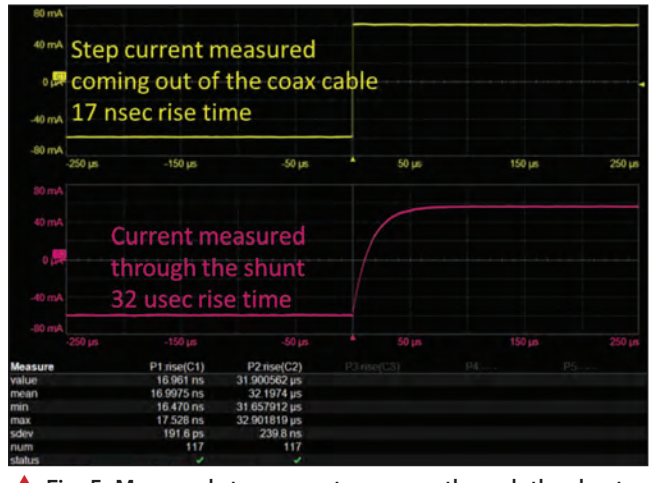

Fig. 5 Measured step current response through the shunt path with a 10-90 rise time of 32 µsec, measured with a Teledyne LeCroy WavePro HD scope.

The transient step response of the current flowing through the shunt path will be a 1-pole response with a pole frequency about 10 kHz. This is an effective RC time constant of about 16 µsec. This would result in a 10-90 rise time of about 32 µsec. This is what is measured in the step response of the current through the shunt path, shown in ***Figure 5***.

Inductively Coupled Noise

In a plane, at frequencies below about 10 kHz, return currents will not flow under the signal path, but will spread out in the return plane. Above 10 kHz, the return currents are localized under the signal paths.

When we have two adjacent signal paths that are over a wide, continuous plane, they will show inductive

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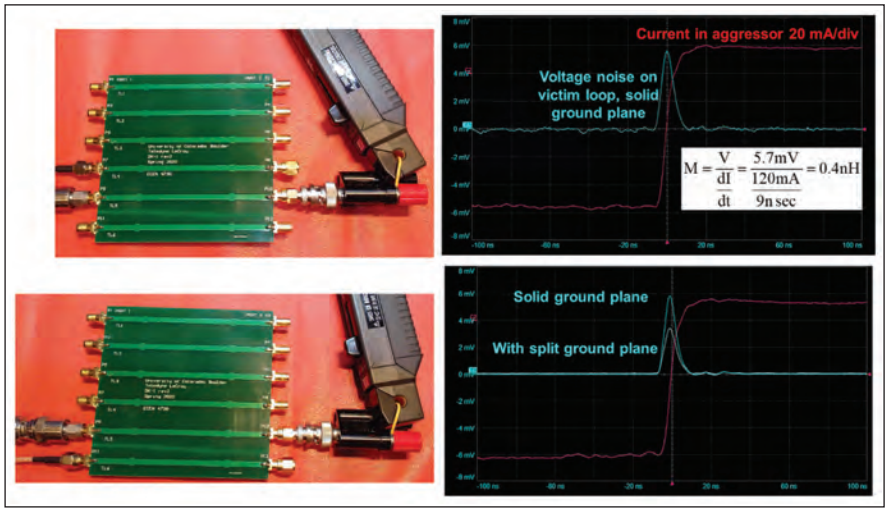


Fig. 6 Measuring the inductively coupled noise on the victim trace adjacent to the aggressor signal with no gap and separated by a gap. The inductively coupled noise is reduced by about 40% on the victim trace separated by a gap. This is a small impact.

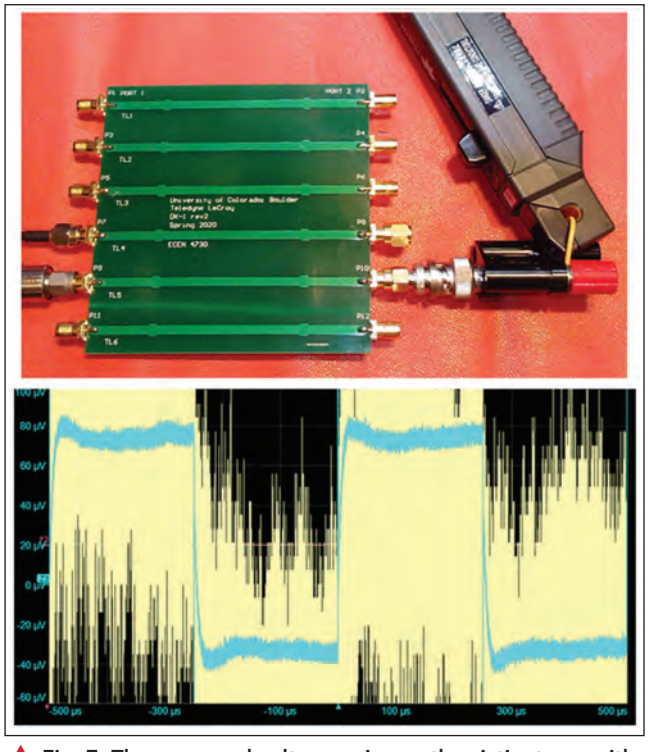


Fig. 7 The measured voltage noise on the victim trace with a scale of 20 μV/div. The raw measurement in one acquisition shows the scope amplifier noise which is reduced with 250 acquisitions averaged together.

crosstalk at high frequency. Even with minimal overlap of the return currents, there is still loop mutual inductance between the two signal-return paths. This inductive noise is driven by the changing current, the dI/dt, in the aggressor signal-return path, that will get smaller at lower frequency.

An aggressor signal with a transient, short rise time current edge will result in a noise signature on an adjacent victim line with a derivative of the aggressor current. The inductive noise would only appear synchronous with the switching current edge. Therefore, we call this sort of inductively generated noise "switching noise," since it only occurs when signals switch transition levels. As the current change drops off with a lower slope, the inductive crosstalk drops off until it is below a measurement threshold.

This behavior was demonstrated in a simple board. In a two-layer board, we constructed six parallel, identical microstrip traces. One was the aggressor. Its far end was shorted to ground. A 2 kHz square wave of 120 mA peak to peak current was transmitted down the aggressor. The rise time was about 9 nsec, but the current was at a constant value for the rest of the period.

There were two victim traces symmetrically on either side of the aggressor. Between the aggressor and one of the victim lines, a gap in the return plane was cut. This isolated the return currents from the aggressor. They were unconstrained to one victim line, but eliminated from flowing under the other victim trace.

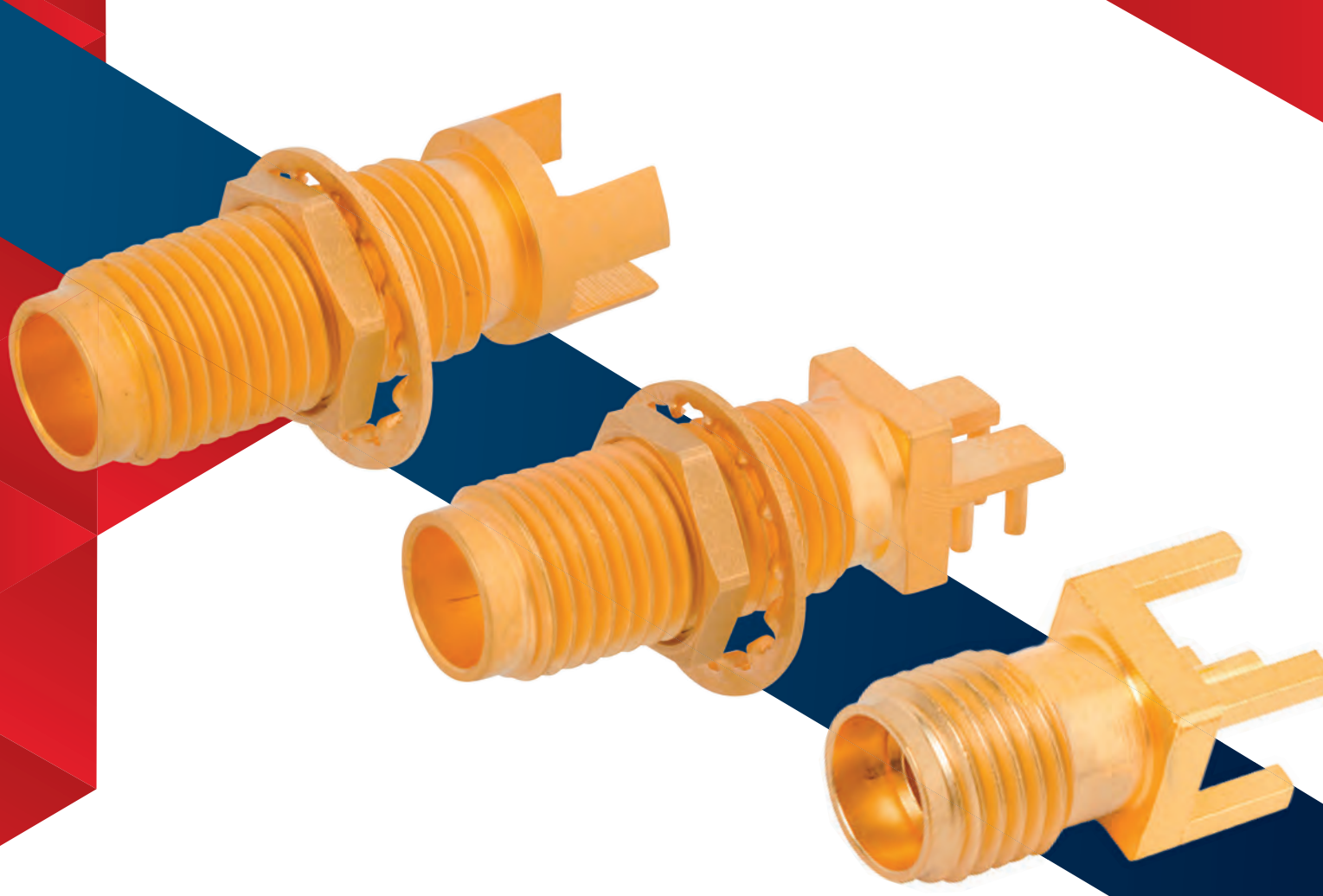
We expect to see switching noise on the adjacent victim trace that lasts only during the 9 nsec of the rise time. The rest of the period should show no switching noise. The measured switching noise on the two victim traces shows the impact from the gap in the return plane. ***Figure 6*** shows the measurement set up of the two configurations and the measured inductively coupled crosstalk on the two victim traces.

We see the signature of the switching noise as the derivative of the current edge. From the measured peak crosstalk (on the order of 5 mV in this example), rise time, and current peak, we can estimate the loop mutual inductance between the aggressor and the victim. With no gap, this is about 0.4 nH of loop mutual inductance. On the other side of the gap, it is reduced to about 0.25 nH. The gap redistributed the return currents and did reduce the loop mutual inductance to the victim trace on the other side of the gap, but it was by a small amount.

Low Frequency Resistive Coupled Crosstalk

At low frequency, when the return currents spread out, they create a voltage drop distribution in the return plane due to the resistance in the plane. With a typical resistance in the return path on the order of 1 mΩ, and currents on the order of 100 mA, this is a voltage drop between one region of the return plane and another on the order of 100 μΩ, for example. This voltage drop, due to the low frequency DC currents on the plane, would appear as a voltage difference between the signal and local return plane on the victim path. It would show up at low frequency and last into DC. However, the magnitude of the resistively coupled noise might be orders of magnitude lower than the inductively coupled noise.

If there were a parallel gap in the return plane between the aggressor and victim traces, the impact



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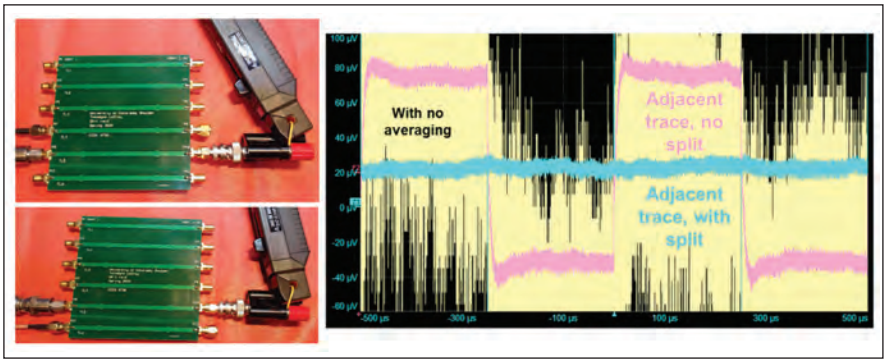

Fig. 8 The measured voltage noise on the victim trace, on the other side of the ground plane gap, showing no resistively coupled cross talk on the order of 10 µV, the noise floor of the measurement.

on the inductive crosstalk would be small. However, the parallel gap would prevent DC currents from the aggressor's return current from flowing under the victim trace and would eliminate the already small resistively coupled crosstalk.

The resistive crosstalk can be measured during the part of the square wave when the current is constant. ***Figure 7*** shows the same measurement of the voltage on the victim trace with no gap between it and the aggressor signal during the entire square wave of current, but on a much higher resolution voltage scale. Note the switching noise that occurs at the edges of the square wave is just visible on this time base scale.

This is a very difficult measurement because the resistively coupled crosstalk is so small. With no averaging, the crosstalk is smaller than the 100 µV RMS amplifier noise of the Teledyne LeCroy WavePro HD, 12-bit scope. To reduce the random noise, we must average consecutive acquisitions, triggering the scope with the function generator's square wave. The random noise decreases with the square root of the number of averages, but the crosstalk synchronous with the function generator stays the same.

We see the very clear DC signature of the resistively coupled noise on the victim trace. Its magnitude is about 120 µV peak to peak. The small offset of about 20 µV is the DC offset of the scope's amplifier. This 120 µV of resistively coupled noise for a peak-to-peak current of 120 mA corresponds to a coupled resistance in the ground plane of about 120 µV/120 mA = 1 mΩ of resistance, or the resistance in about 2 squares of ground plane for this board.

This 120 µV of resistive noise is due to the overlap of the return currents of the two conductors, roughly 1 in. apart, with 120 mA of aggressor current, passing through the 1 mΩ of overlapping plane resistance. This is the crosstalk noise we would want to eliminate with a split ground plane.

A Split Ground Plane Eliminates DC Resistively Coupled Noise

When we cut a gap in the return plane, there will be no DC current flow across the gap. There will be magnetic field coupling across the gap, which is why we still see significant mutual inductance coupling between the aggressor and victim across the gap. The gap has only a small impact on this noise.

However, we would expect there would be no resistively coupled noise on the victim trace on the other side of the ground plane gap. In ***Figure 8***, the resistively coupled noise is measured with the same scale and averaging as the noise on the victim line with no gap. The noise floor of this measurement is about 10 µV. To

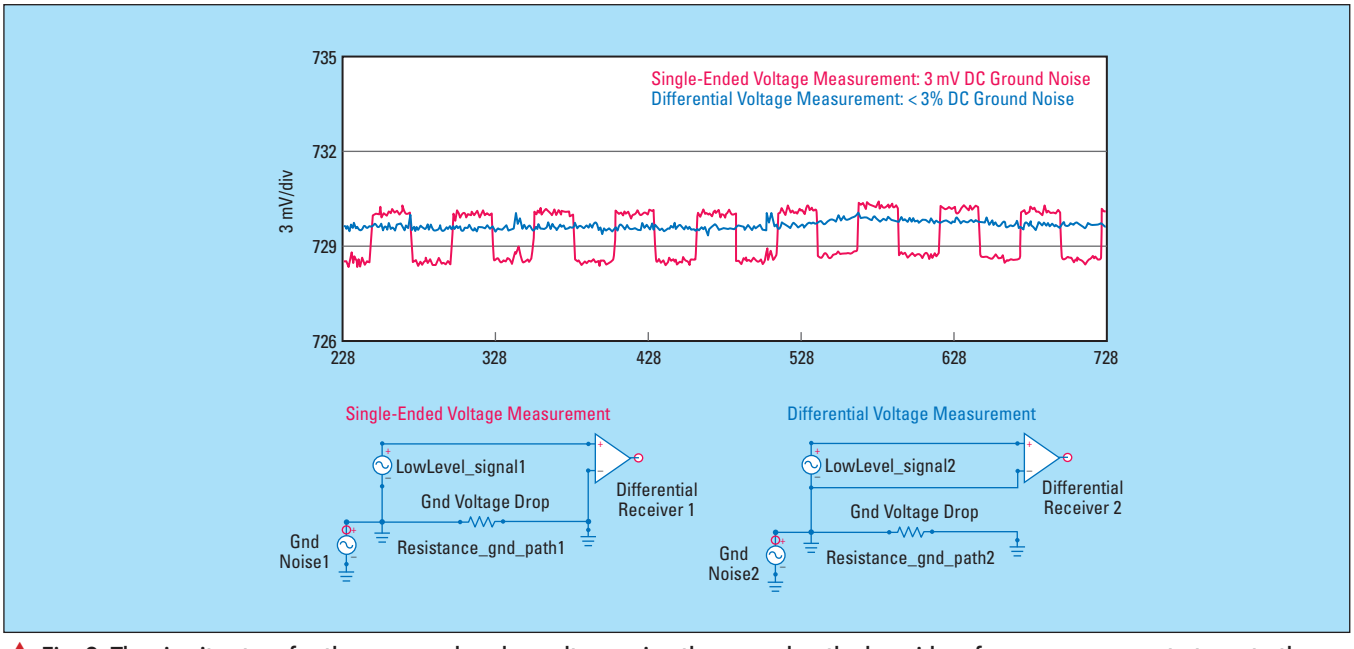

Fig. 9 The circuit set up for the measured analog voltage using the ground as the low side reference or a separate trace to the differential input. The measurements on the right show the ground noise on the signal ended signal, but no impact on the differential measurement.

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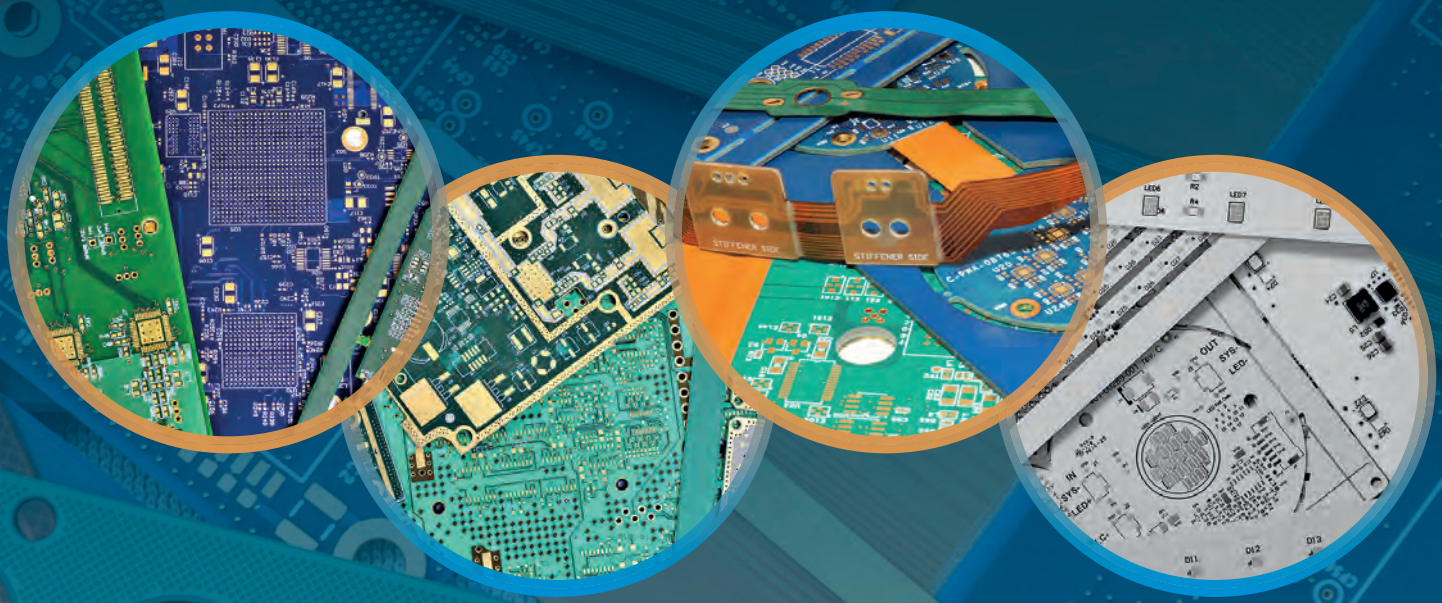

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this level, there is no measurable resistively coupled noise, a significant reduction.

There is still inductively coupled switching noise that lasts for the rise time of the square wave, about 9 nsec. This noise is just barely visible with this time base of 100 μsec/div. It is the initial spike at the edges of the square wave.

It is this small amount of resistively coupled crosstalk that a gap in the ground plane would prevent. It keeps the DC currents, which will spread out from the signal paths, from flowing in the ground plane to induce a DC offset noise in the return path of other signals.

Generally, this amount of noise will be on the order of 100 μV, corresponding to 100 mA flowing through 1 mΩ of coupled resistance. In an ADC with a 5 V reference and 15-bit resolution (plus sign), 1 bit would be a voltage level of about 5 V/32,000 = 150 μV. The DC coupled ground plane voltage noise could contribute about 1 least significant bit level. Fluctuations in the 100 mA of ground currents, could be at the sensitivity level of a 16-bit ADC in some cases. It would be noticeable in a 24-bit ADC.

One solution to reduce this noise would be to isolate either the high current paths or the sensitive signal paths using an isolating gap in the return plane, parallel with the signal conductors, to make sure no signals cross this isolating gap. This is the problem solved by a gap in the return plane.

If there are 100 A of DC current flowing, the ground plane noise could be 100 mV or more, but other design considerations such as thicker copper, more ground planes, and placement of the VRM in proximity to the load must be considered.

While a gap in the return plane would dramatically reduce the resistively coupled noise on analog signals where voltage noise on the order of 100 μV was important, there is a more effective way of reducing this sort of common noise on sensitive signals that is also robust and does not run the risk of inadvertently having signals cross the isolation gap.

Differential Signaling Also Eliminates the Resistive Coupled DC Crosstalk

Most applications that are sensitive to 100 μV of low frequency noise involve measuring low level signals from sensors or microphones. An important design guideline when measuring these sorts of voltage sources is to use a differential measurement.

If the sensor itself generates a differential signal or even a single-ended signal, you would route a separate trace for both the high and low ends of the sensor, back to a differential receiver, such as an instrumentation amplifier. Even if the sensor is single-ended, the ground connection to the sensor's low side could be connected at only one point, either at the sensor or at the input to the differential receiver, rather than both ends.

The voltage difference between the high and low side of the sensor is brought back to the input of the differential receiver, without using the ground plane, which might have the common DC voltage drop coupled noise in it. This separate dedicated low trace

would not have the DC current of the return plane traveling in it.

This principle is illustrated in a simple experiment. A TMP36—a voltage sensitive temperature sensor—was used as the sensor. At room temperature, it generates a DC voltage of about 730 mV. It is a single-ended signal.

The output of this sensor was measured with a differential amplifier and a 16-bit ADC using the ADS1115. It was measured in two configurations, with the low side connected to the ADC using a common ground path, and with a separate return line connecting the low side of the sensor to the low side input of the ADC.

While these measurements were being made, a 1 Hz square wave of current was passed through the common return path. The common resistance was increased to accentuate the coupled noise. When the 100 mA of ground current was sent through the ground path, a noise level of about 2 mV was generated in the ground path from the sensor to the ADC. This voltage noise appears in series with the low level sensor voltage when the return path is used to connect the low side reference.

When the low side reference is carried in a separate, isolated trace, there is no impact on the differential signal from the DC noise in the return path. This result is shown in ***Figure 9***.

The differential signal path from the sensor to the differential receiver does not have the voltage drop of the ground plane in its path. The measured signal does not show any of the DC resistive crosstalk in its signal. This is the way to route sensitive analog signals, so they are not sensitive to very slight resistive crosstalk from low level signals.

Conclusion

The problem a split in the ground plane solves is reducing the very small low frequency resistive crosstalk of return currents which spread out. This typically arises at frequencies below 10 kHz and is equivalent of a common, shared resistance on the order of a few squares of sheet resistance, on the order of 1 mΩ.

If your application has very low level analog signals that must be routed across a board and might be sensitive to these low level sources of low frequency noise, a better solution is to use differential signal routing and a differential receiver.

The risk of adding a split in the ground plane to fix this very small problem is the possibility of higher bandwidth signals inadvertently crossing this gap. This can result in a pathological problem which will easily cause a board to fail in several ways.

Except in the simplest of boards, the risk from including a gap in the return path strongly outweighs the potential benefit. Carefully consider your engineering rationale to add a split in the ground plane, and to reduce risk, consider alternative solutions.■

Avoiding GIGO with Field Solvers

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To avoid "garbage in, garbage out" (GIGO) with any field solver, first you need to understand the little nuances of PCB fabrication processes and how to interpret manufacturers' data sheets. But most importantly you need to understand the tool's user interface and what it is asking for.

All 2D or 3D field solvers will give accurate impedance predictions. The differences are the type of solvers used under the hood and complexity of the user interface. Simple 2D field solvers, used in many of today's stackup planners, simply give predicted characteristic impedance based on material properties and trace geometries. More complex, 2.5D or 3D field solvers, allow for additional material parameters and can also predict insertion loss, phase delay, and impedance over frequency. Some will even export RLGC and touchstone S-parameter files for further signal integrity analysis.

Standard PCBs are fabricated using cores and prepreg material. Prepreg sheets are a mixture of fiberglass (glass) cloth and resin which is partially cured. Cores are simply cured prepreg sheets with copper bonded to one or both sides of the laminate. Copper is etched away on each side of the foil to leave the circuit pattern.

In a multi-layer PCB, cores and prepreg sheets are alternately stacked symmetrically above and below the middle of the layup then pressed under heat and pressure. The prepreg layers get thinner when pressed allowing the resin to fill the voids between the copper features that were etched away on the cores.

One important parameter for accurate impedance modeling is dielectric constant (Dk). The best source is from laminate sup-

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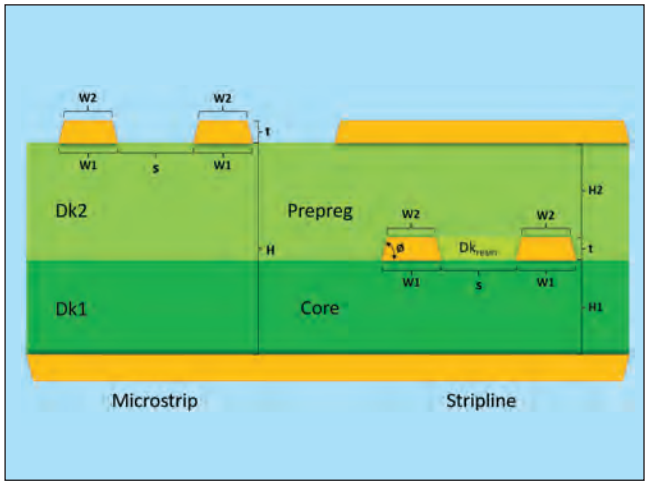

Fig. 1 Generic microstrip and stripline geometries.

pliers' data sheets. But all data sheets from laminate suppliers are not the same.[3]

"Marketing" data sheets are data sheets easily found on laminate suppliers' websites. They are meant for a quick comparison of dielectric properties to narrow your search for the right laminate for your application. They include mostly thermal and mechanical properties, which are important for the physical structure of the material and how it will perform with other material properties in the stackup during processing.

Marketing data sheets usually only report a typical Dk value at 50% resin content at two or three frequency points. Depending on glass style, resin content and thickness, Dk and dissipation factor (Df), will be different for different cores and prepreg thicknesses for the same laminate chemistry. In the end, they are not representative of what is needed to design an actual stackup, or to do impedance and loss modeling. Using these numbers will almost always lead to inaccurate impedance and signal integrity (SI) results.

Instead, you need to use the same Dk/Df construction table data sheets that PCB fabricators use for the stackup. Dk/Df construction tables provide the actual core and prepreg thicknesses, resin content, and Dk/Df for the different glass styles, over different frequencies. Depending on the stackup, a combination of thicknesses is often needed to meet impedance requirements and have different Dk values.

Many engineers assume Dk published is the intrinsic property of the material. But in fact, it is the effective Dk (Dkeff) measured by a specific industry standard test method. It does not guarantee the values directly correspond to design applications. When compared against measurements from a design application, there is often a discrepancy in Dkeff due to increased phase delay caused by surface roughness.[1]

Dkeff is highly dependent on the test apparatus and conditions of how it is measured. One popular test method, IPC-TM-650 2.5.5.5C clamped stripline resonator test method, assures consistency of product during fabrication. Due to the nature of this test method, the materials under test are not physically bonded together, air is entrapped between the various layers. These

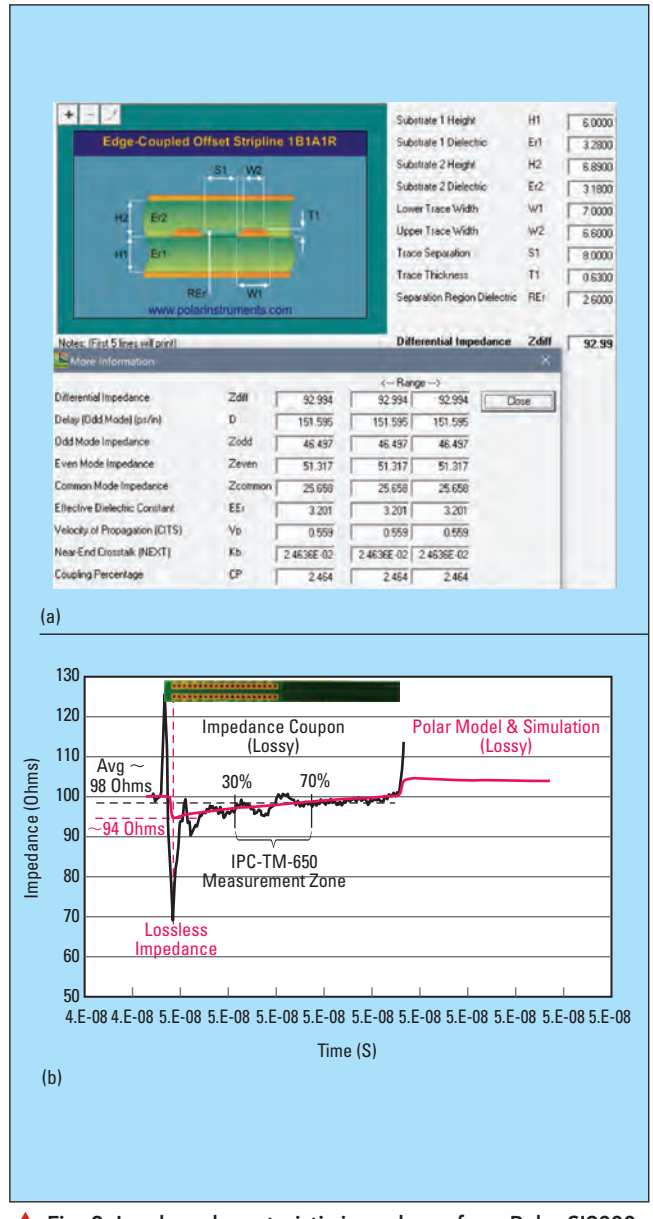

Fig. 2 Lossless characteristic impedance from Polar SI9000 field solver (a) vs. measured TDR plot from an impedance coupon and lossy transmission line model from Polar Si9000 (b).

small air gaps are caused by: roughness of the copper foil plates in the fixture, roughness profile imprint left on the surface from the foil that was removed from the test samples, and copper removed on the resonant element pattern card. Air entrapment results in a lower Dkeff than what is measured because in a real PCB everything is bonded together, with no air entrapment.[3]

All glass weave reinforced laminates are anisotropic, which means E-field orientation, relative to the glass weave, is different depending on test method. E-fields produced from tests like IPC-TM-650 2.5.5.5C are transverse to the glass weave and Dkeff measured is out-of-plane.

E-fields produced by TM-650-2.5.5.13 split post cavity resonators are parallel to the glass weave Dkeff measured this way is in-plane. Dkeff is typically higher for in-plane measurements, compared to out-of-plane,

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depending on the glass resin mixtures used in the stackup.

Another source of discrepancy is not accounting for increased Dkeff due to the pressed thickness of prepreg. Since prepreg sheets have a certain percentage of resin content for the thickness, after pressing the resin content is reduced and since Dk is a function of resin and glass mixture, there will be a higher percentage of glass after pressing and thus slightly higher Dkeff.

The most common PCB trace geometries are microstrip and stripline. A simple microstrip geometry is bare copper traces over a reference plane, separated by a dielectric height H, as shown in ***Figure 1***. Depending on the stackup, there may be a core and prepreg layer between the outer layer and reference plane with the same or different Dk values for Dk1 and Dk2.

Simple stripline geometry has copper traces between two reference planes. For single-ended (SE) signals, there is only one trace used in the field solver to calculate the SE impedance. For differential pairs, there are two traces separated by a space. Because resin fills the voids between copper features the Dk_{resin} will be lower than Dk1 or Dk2, shown in Figure 1.

The last thing to note is the wider side of the trace always faces the core material. This is a very important point to remember when using any field solver. If you get it reversed, it will lead to inaccurate results.

The thickness of copper traces is an important parameter for accurate impedance prediction. Copper thickness is usually specified in ounces per square foot. Most common thicknesses for inner layer traces are ½ and 1 oz foil. But field solvers expect an actual thickness dimension.

Most designers assume 0.7 mils (18 μm) thickness and 1.4 mils (36 μm) for ½ and 1 oz, respectively. But because of the price of copper, the copper you get from foil manufacturers will likely be the minimum thickness allowed under IPC-4562A. When you factor in the typical thickness after fabrication, the typical thickness can be 0.6 mils (15 μm) and 1.2 mils (30 μm). But the minimum thickness allowed under IPC-A-600G-3.2.4 is 0.45 mils (11.4 μm) and 0.98 mils (24.9 μm) for ½ oz and 1 oz, respectively.

Due to the nature of the etching process, the traces will usually be trapezoidal in shape. This is known as the etch factor (EF), as defined by IPC-A-600G. It is the ratio of the thickness (t) to half the difference between W1 and W2, shown in Figure 1.

Thus,

$$\text{EF angle } (\emptyset) = arctan\left(\frac{t}{0.5(W1 - W2)}\right)$$

Some field solvers will define EF differently, so it is important to understand how to specify it properly.

Once you've come up with a proposed stackup, the next step is to do some impedance modeling. Normally your fab shop comes up with this, but it is a good idea to validate their proposal, to ensure you are in sync with them.

The first thing to do is identify the layers from which to model. Next, use your field solver to model characteristic impedance. Since all field solvers are different, and user interfaces can be confusing, make sure you understand the little nuances of your tool.

The next thing is to identify the core layers in the stackup and input H1 and Dk1 for the dielectric. Then, input the pressed thickness for prepreg H2 and Dk2, not the thickness found in Dk/Df construction tables. But be careful how the field solver defines H2. Most field solvers define it as shown in Figure 1, but some solvers, like Polar Si9000e, define H2 as the thickness of prepreg plus thickness of trace (H2+t), shown in ***Figure 2***. Usually, you can trust the pressed thickness from your board shop stackup drawing.

Finally, if your field solver allows for it, fill in Dk_{resin} between two traces if you know it. It will be lower than Dk2. Since this number is generally hard to obtain, a rough estimate to use is the lowest Dk value from the highest resin content prepreg found in Dk/Df construction tables. Once everything is set up, optimize the line width and space until the desired characteristic impedance is reached.

One last point to remember is that all 2D field solvers only calculate the lossless characteristic impedance. But when we measure an impedance test coupon with a time domain reflectometer (TDR), we are measuring the instantaneous impedance of a lossy transmission line at every point along its length. More often than not, impedance is different than what was predicted.

A 2D field solver has no input for conductor resistivity, dielectric loss, or the length of the conductor. Resistive loss often results in a slow monotonic rise in the impedance profile. IPC-TM-650 specifies the measurement zone between 30% to 70% and most PCB fab shops will measure an average impedance.

In the example, shown in Figure 2, for a low loss dielectric there is a 4 to 5 Ohm difference depending on where the measurement is taken. When all input parameters are included correctly for a lossy transmission line model, you can see there is excellent correlation.

Although minor differences in individual parameters may have second order affects, collectively they could add up to give poor correlation to measurements. But if you consider all the nuances discussed in this article, you can get pretty good accuracy as shown in Figure 2.■

REFERENCES

1. B. Simonovich, "A Practical Method to Model Effective Permittivity and Phase Delay Due to Conductor Surface Roughness", *DesignCon, 2017*.
2. B. Simonovich, "PCB Fabrication: What SI/PI Engineers Need to Know for First Time Modeling Success", *DesignCon 2021 Spring Break Webinar*, April 12, 2021.
3. B. Simonovich, "A Tale of Two Data Sheets and How Foil Roughness Affects Dk," White Paper.

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Selecting a Backplane: PCB vs. Cable for High-Speed Designs

Andrew Josephson, Brandon Gore, and Jonathan Sprigler
Samtec, New Albany, Ind.

As with any design decision, selecting a backplane design approach requires tradeoffs in price, flexibility, and performance specific to a particular network topology. This article analyzes the effect on high-speed serial-link performance for a printed circuit board (PCB) backplane versus a backplane constructed of connectorized cable assemblies, particularly in terms of IEEE and OIF compliance specifications, and notes what kinds of applications might be well suited for a cable or PCB backplane.

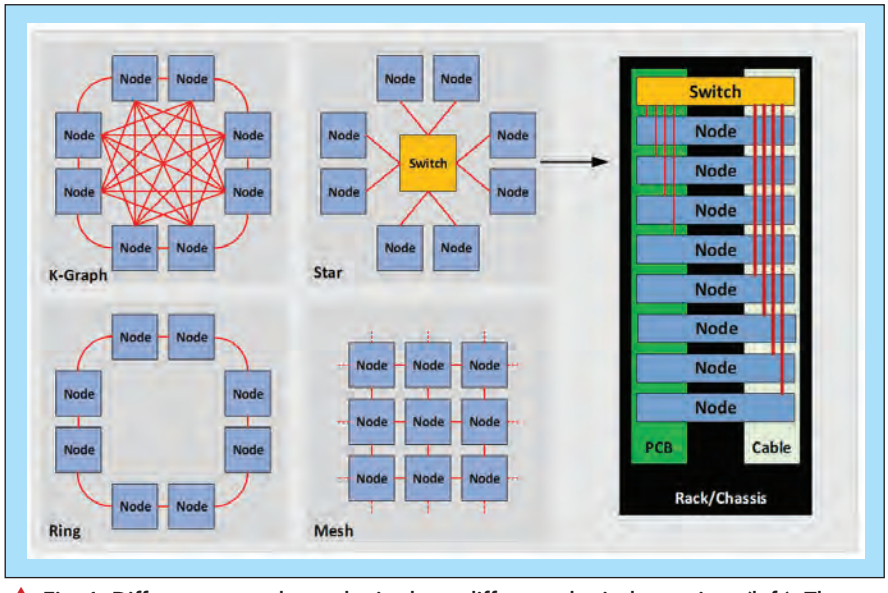

Fig. 1 Different network topologies have different physical mappings (left). The "star" configuration is perhaps the most common, but there are many applications also using K-graph, ring, and mesh topologies. The star topology is detailed in a flat representation of a rack/chassis, showing where one might use PCB backplane versus cable in a mix-and-match configuration (right).

Should I use a cable or PCB backplane in my system design? As with most questions regarding signal integrity, the answer is: it depends. In this article, we take a close look at signal integrity implications at the component and system levels for applications that require a backplane, noting performance opportunities as well as integration tradeoffs and advantages.

At the BOM level, a cable backplane can be more expensive than a traditional PCB backplane. But, at the system level, it can offer significant advantages by enabling earlier software development and integration activities in the front end and lower total cost of ownership on the back end. For instance, a cabled backplane can offer the flexibility to interface blades with test equipment,

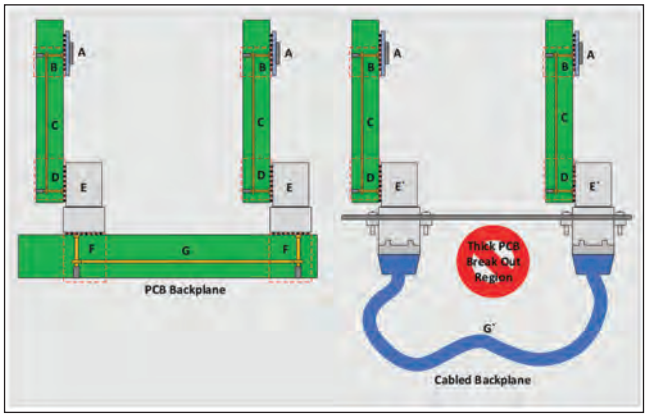

Fig. 2 Comparison of a PCB backplane topology vs a cabled backplane topology; all of the components are identical up until the mated connector. The analysis in Figures 3 and 4 are based on this model, comparing what occurs after the signal gets to the module connector (E and E').

software development platforms, and early engineering prototype systems, all while offering high enough performance to futureproof the production solution. Additionally, the improved channel performance, or reach, with cable assemblies as compared to PCB routes can be used in some case to increase network spans and physically reach more nodes.

Figure 1 shows physical mappings for several common network topologies. In the case of the star topology outlined in the rack/chassis in the right side of the figure, the node or blade can be the same design with the same connectors, regardless of whether it has a cable or PCB backplane. As a result, it is possible to design for a PCB backplane today and migrate to a higher-speed cable backplane later, or design for a cable backplane today to achieve extra margin. This would allow for insertion of new blades and switches in the chassis later, netting substantial design and system reuse. When used as an Agile systems integration on/off ramp and potential product life cycle extender, the upside opportunities offered with cabled backplane approaches can vastly outweigh differences in component cost.

In the case of the simple ring, mesh, and star topologies (Figure 1), using a cable backplane might allow the nodes to be populated at an increased blade or module pitch (accommodating thermal design space as component power densities increase, or potentially placed in adjacent racks or chassis). Depending on the distance from the switch, when PCB loss becomes limiting, migration to cabled backplanes can be easy.

In more complicated network topologies with many more segment crossings, cabled backplane approaches can run into scaling issues, making PCB route approaches more attractive. Additionally, PCB-based backplanes can offer advantages for co-design with other infrastructure, such as power delivery and out-of-band low speed signals.

Backplane Performance

In terms of performance, both PCB and cable backplanes can offer excellent performance at shorter channel links, while cable backplanes enable excellent signal speeds also at longer channel links. One reason cable backplanes can do this is that the traces are not running through the PCB, so each of the differential pair can go through an individual shielded cable. This can lead to less loss and better signal integrity vs. a PCB channel.

Figure 2 shows the models for a PCB backplane topology vs. a cable backplane topology, using the same BOM (see ***Table 1***) except for the cable and the PCB backplane. The significant difference between the two topologies is the loss per unit inch between a PCB backplane (G) and a cabled backplane (G'). In this model, at 26.56 GHz (IEEE 802.3ck 400GBASE-KR4 signaling frequency), the loss for G is designed to 1.0 dB/in., and the loss for G' is 0.25dB/in.[1] Of course, there is also no PCB backplane connector vias and break out areas in the cabled backplane model, and these can be areas of significant signal integrity degradations in the channel.[2]

Figure 3 shows the modeled and simulated insertion loss between the topologies, described in Figure 2, with two different length options for each type of topology. The significant change is the loss between the pink traces (PCB backplane 2 and 16 in.), with the most loss in the 16 in. PCB backplane channel still providing approximately 6 dB of insertion loss margin. But is that

TABLE 1

BOM FOR FIGURE 2 - NOTE THESE SHOULD BE THE SAME CONNECTORS, BUT THEY ARE DESIGNATED DIFFERENTLY BECAUSE OF WHAT THEY MATE TO.

Item	*Description*
A	COM Package Model
B	1 mm BGA PTH BOR (8 mil Backdrill Stub)
C	3" 92.5Ω T-Line (1.2 dB/in. at 26.56 GHz)
D	Module/Blade PTH Connector BOR (8 mil. Backdrill Stub)
E	Mated RA to BP Samtec Connector
F	Backplane Connector PTH BOR (8 mil. Backdrill Stub)
G	2" to 16" Variable 92.5Ω T-Line (1.0 dB/in. at 26.56 GHz)
E'	Mated RA to Cable Samtec Connector
G'	4" to 16" Variable Samtec 92.5Ω TwinAx Cable (0.25 dB/in. at 26.56 GHz)

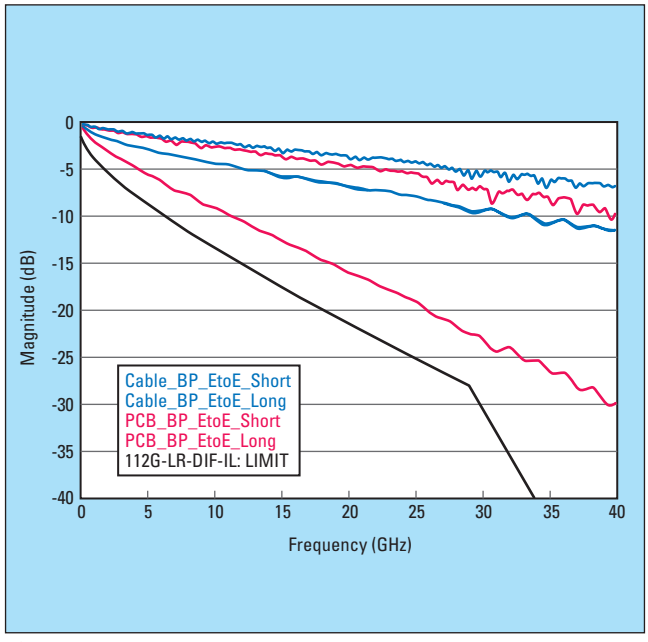

Fig. 3 A comparison of insertion loss for 4 and 18 in. cables (blue traces) and 2 to 16 in. PCB backplanes (pink traces). The black line shows the industry standard insertion loss limit. All options work within the design parameters out past 35 GHz, and they offer a 5 or 6 dB design margin, which traditionally has been enough to accommodate loss issues in the system design.

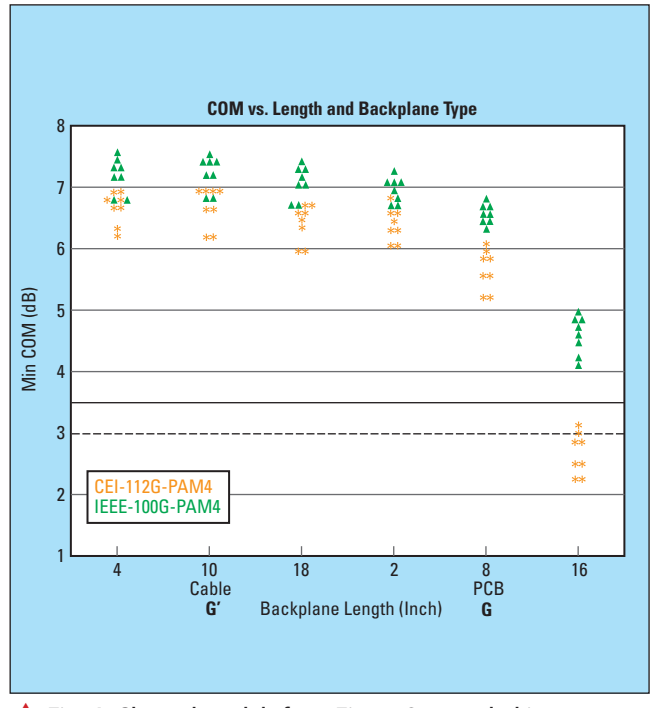

Fig. 4 Channel models from Figure 3 extended into an 8-lane design, with each lane acting as victim while all other lanes act as near-end transmitting aggressors. The three models on the left are for cable backplane, and the three on the right use a PCB backplane. Note that the 16 in PCB backplane channels (which had 5 dB insertion loss margin in Figure 3) now have negative margin for COM system level metrics on most 112G lanes.

enough? Answering this requires performing system level channel analysis.

System Level Channel Analysis

When eight lanes are plotted, assessing system level losses against PAM4 requirements using channel operating margin (COM), things do not feel quite as safe (see ***Figure 4***). Higher data limits, such as CEI-112G-LR-PAM4[3] and IEEE 802.3 400GBASE-KR4,[4] lead to loss of margin at the system level, especially when designing systems for cost effectiveness.

In this model of 800 GbE ports, each lane acts as a victim while the seven other lanes act as near-end transmitting aggressors. In Figure 4, the green points are at CEI-112G-LR-PAM4 while the orange are at IEEE 802.3 400GBASE-KR4; the three plots on the left are for cable backplane (G') while the three on the right are PCB backplanes (G).

We would expect to have less margin with the higher data rates, and that is supported in this graph. Note that 4 in. of cable backplane has very similar performance to 2 in. of PCB backplane. The cable backplane demonstrates similar COM performance across all three lengths (4, 10, and 18 in.) while the PCB backplane exceeds the ability of the SERDES to compensate for loss, reflections, and crosstalk after 8 in. of backplane route length. In addition, for the 8 and 16 in. PCB backplane, note the delta between 100G and 112G speeds with the separation in COM results becoming more pronounced. For a 16 in. backplane at 112G PAM4, this system has a negative COM, despite having significant margin with respect to the OIF-CEI-112-LR insertion loss limit line.

In the past, the 6 dB margin demonstrated in Figure 3 would be a comfortable place for the designer to stop development and analysis, confident that unaccounted for error terms would be small in comparison. For 112G and higher, that is no longer the case and channels must be assessed with true end-to-end multi-lane effects at the system level including all significant regions of interconnect. Connector systems that offer options for both board-to-board and cable-to-board interconnects can be used to navigate the design trade space and offer significant opportunities for earlier integration and longer sustainment.■

REFERENCES

1. Samtec Twinax Product Data, Web: https://www.samtec.com/s2s/system-optimization/twinax-flyovers/.
2. B. Simonvich, "Controlling Electromagnetic Emissions from PCB Edges in Backplanes," *Signal Integrity Journal,* January 2017, Web: https://www.signalintegrityjournal.com/articles/292.
3. Optical Internetworking Forum, "Common Electrical I/O (CEI) - Electrical and Jitter Interoperability agreements for 6G+ bps, 11G+ bps, 25G+ bps, 56G+ bps and 112G+ bps I/O," Implementation Agreement OIF-CEI-05.0, May 2022, pp. 582-597. Web: https://www.oiforum.com/wp-content/uploads/OIF-CEI-5.0.pdf.
4. The IEEE 802.3ck Taskforce, Web: https://www.ieee802.org/3/ck/index.html.

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Power Integrity Testing Requirements Introduce Extreme Interconnect Measures

Steven M. Sandler
Picotest, Phoenix, Ariz.

Power Integrity (PI) engineers are familiar with the ground shield effect in the 2-port shunt-through measurement. If not, there are many papers, articles, and videos on the subject.[1,2] PI engineers are less knowledgeable about the impacts on other power-related measurements. In this article, we focus on power supply rejection ratio (PSRR), power supply modulation ratio (PSMR), and power supply noise rejection (PSNR) measurements, which are all measures of how power rail noise appears at the output of voltage regulators, RF amplifiers, and digital channel jitter.[3]

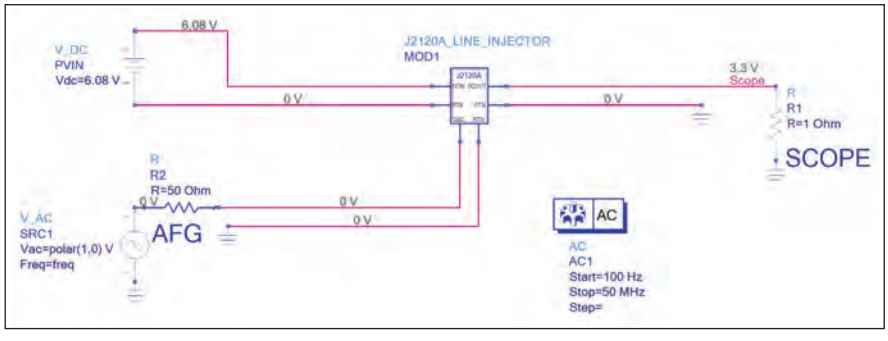

Fig. 1 A simplified setup schematic for a PSRR/PSMR/PSNR measurement using the Picotest J2120A line injector. This setup is showing just the modulation signal, as seen at the 1 Ohm load.

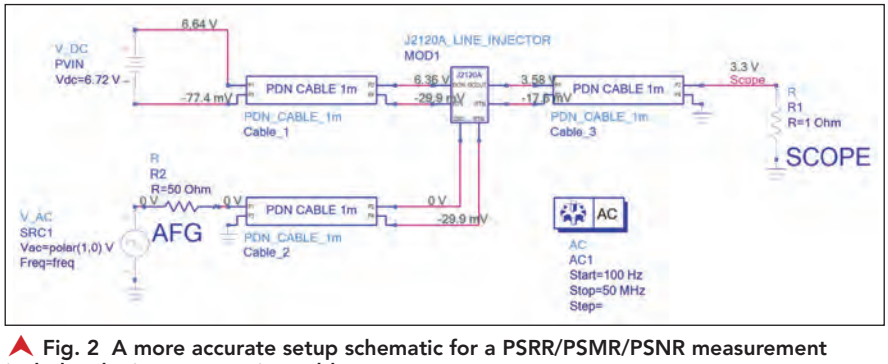

Fig. 2 A more accurate setup schematic for a PSRR/PSMR/PSNR measurement includes the interconnecting cables.

Modulation

A simplified schematic of a typical PSRR/PSMR/PSNR measurement test setup is shown in ***Figure 1***. The measurement requires a modulation signal to be superimposed on the DC power rail. This can be almost any noise source that you want to impose on the input bus voltage going to the device under test (DUT). There are several ways to accomplish this, but this schematic shows a typical line injector. An external voltage source is connected to the line injector power input, which includes significant decoupling. A signal generator provides the modulation via the modulator input, and the AC (noise) and DC are mixed in the line injector and provided at the line injector output. Normally the noise voltage is recorded at the output of the DUT to see what portion of the noise is transferred from the input of the DUT to its output downstream. The schematic assumes that the modulation input is internal to the oscilloscope and therefore shares the same RF ground at the oscilloscope. The oscilloscope is monitoring the signal at a 1 Ohm load resistor.

A more accurate representation includes the interconnecting cables as shown in ***Figure 2***. This setup is showing just the modulation signal,

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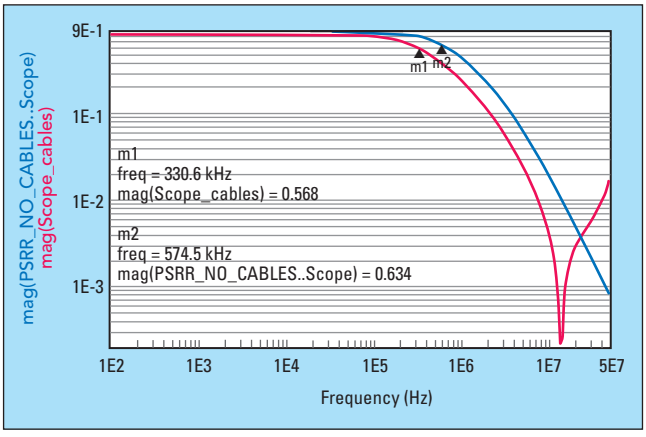

Fig. 3 The modulation signal is monitored at the 1 Ohm load resistor. The addition of the interconnecting cables has a significant impact on the bandwidth of the modulation signal and the interconnecting cables also introduce a sharp resonance just above 10 MHz.

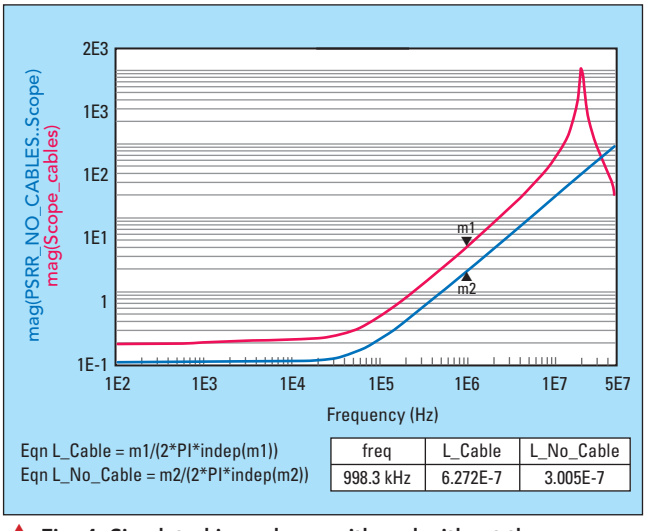

Fig. 4 Simulated impedance with and without the interconnecting cables. The interconnecting inductance is more than doubled because of the interconnecting cables.

as seen at the 1 Ohm load. Note that the benchtop power supply voltage had to be increased by 640 mV to account for the cable voltage drops in order to produce 3.3 V at the output side. This schematic includes 1 m cables, though this is a somewhat arbitrary choice, as is the selection of the cable connector type.

The modulated signal at the load resistor is shown both with and without the interconnecting cables in ***Figure 3***. There are four interesting observations in the resulting simulations. First, the addition of the cables attenuated the modulation signal by about 9%. Second, the bandwidth of the modulated signal is reduced by 42%. Third, both modulation signals are significantly attenuated by several MHz. Finally, the addition of the cables introduced a sharp resonance just above 10 MHz.

The impedance of the modulation signal at the load resistor is also simulated for these two cases—with and without the interconnecting cables. The impedance results are shown in ***Figure 4***. The interconnecting cables more than doubled the inductance of the interconnect as seen at the load.

TABLE 1

SUMMARY OF THE POWER SUPPLY MODULATION SIGNAL REQUIREMENTS IN THE QSFP-DD REV 6.2 SPECIFICATION

Note the testing requires a bandwidth of 40 Hz to 10 MHz

Power Supply Output Noise and Tolerance Specifications					
Parameter	***Symbol***	***Min***	***Nom***	***Max***	***Unit***
Host RMS noise output 40 Hz -10 MHz (eN_Host)[1,3]				25	mV
Module RMS noise output 40 Hz -10 MHz[2,3]				30	mV
Module sinusoidal power supply noise tolerance 40 Hz -10 MHz (p-p)[2,3]	$PSNR_{mod}$			66	mV

Why This Matters

New, higher speed devices require testing to much higher bandwidths than the results of either of these simulations. Consider the new QSFP-DD Rev 6.2 PSNR requirement for the QSFP Double Density 8× and QSFP 4× pluggable transceivers. A summary of the modulation requirements is shown in ***Table 1***.

This new specification requires a signal injection of up to 10 MHz, while some PLL applications require modulation signals of up to 50 MHz.

Consider the QSFP-DD Class 7 Requirement, which defines the power rail voltage as 3.3 V and the operating current as 5.6 Amps. The equivalent load resistance is:

$$Rload = \frac{Vcc}{Icc} = \frac{3.3\ Volts}{5.6\ Amps} = 0.59\Omega \quad (1)$$

The 3 dB modulation bandwidth impact, due to the interconnect, is defined by the frequency at which the interconnect impedance is equal to the load impedance:

$$Bandwidth = \frac{Rload}{2\pi \cdot L} \quad (2)$$

Where L is the interconnecting inductance of the power rail seen at the load. Solving for the allowable interconnect inductance

$$L = \frac{Rload}{2\pi \cdot Bandwidth} = \frac{0.59}{2\pi * 10\ MHz} = 9.39\ nH \quad (3)$$

The required interconnect inductance is much lower than the Picotest J2120A line injector can provide, even without the cables included. The addition of the cables exacerbates the situation.

Parallel wires, close together, result in an inductance of about 10 nH/inch.[4] This is shown in ***Figure 5***. Achieving a 9.4 nH interconnecting inductance, assuming the modulator itself introduces near-zero inductance, requires that the modulation signal be less than 1 in. from the transceiver being tested. A passive line injector with a voltage drop of approximately 2 V, and an operating current of 5.6 Amps, dissipates a power

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Fig. 5 Many online calculators are available for determining the inductance of parallel wires: This example shows the total inductance of a pair of 1 in. long, 31 mil diameter wires, spaced 50 mils apart. Spacing the wires 100 mils apart will approximately double this inductance.

of 11.2 W. The line injector itself also needs to offer a bandwidth greater than 10 MHz. Together these requirements present a significant challenge.

Creating a Solution

Considering these three challenges:

- Improve the output bandwidths for injected noise to > 10 MHz
- Place the modulator (line injector) within 1 in. or less of the DUT
- Thermal design to support 11.2 W.

Achieving the bandwidth is made possible by utilizing small eGaN semiconductor devices in place of Si. These very small eGaN devices are extremely fast due to very low junction capacitance combined with very low internal resistance.

Reducing the device size along with some other design changes allows the circuit to be miniaturized to the point that the line injector form factor can be a very small form factor probe.

Dealing with the thermal issues is the most challenging task. Placing the device in a small probe allows the line injector to get very close to the device under test. The small form factor also prohibits the use of passive cooling solutions, which would be quite large. The thermal issue is resolved using a very small, precision micro-machined liquid cooling system (see ***Figure 6***).

The modulation bandwidth required by the QSFP-DD Rev 6.2 specification is 66 mV rms from 40 Hz to 10 MHz. The 3 dB frequencies are shown in ***Figure 7***, with a lower frequency point at 35 Hz and an upper frequency point at 40 MHz. Two points are added at 10 and 100 kHz to show the midband flatness.

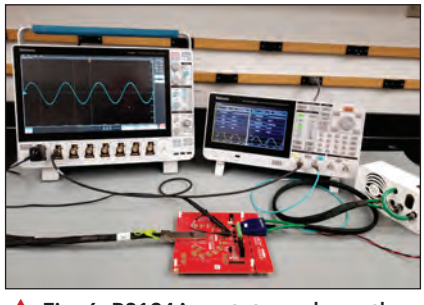

Fig. 6 P2124A prototype shows the electronics module and GaN cooling mechanism. The cooling pump is the white box tucked between the scope and signal generator (courtesy of Molex).

Though the signal is attenuated at higher frequencies by the interconnect wire inductance and the transceiver resistance, it is possible to modulate at 250 MHz, or higher, as shown in ***Figure 8***.

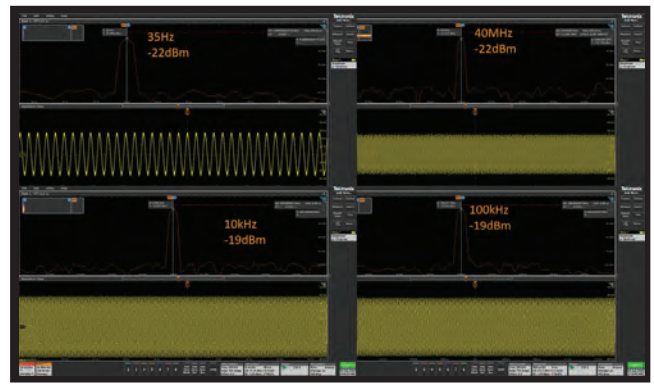

Fig. 7 Modulation at 10 MHz is flat with a 3 dB point at 40 MHz with short interconnect wires. The QSFP-DD specification requires a bandwidth of 40 Hz to 10 MHz.

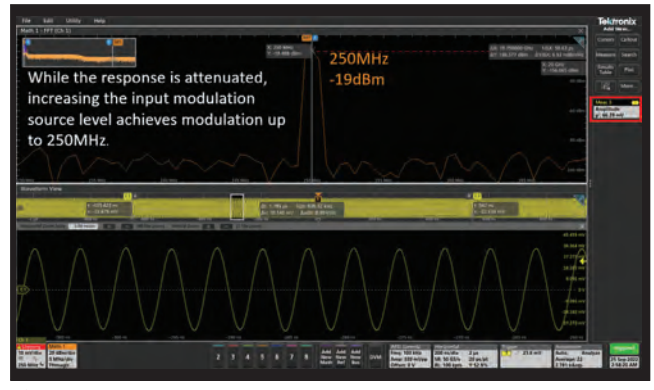

Fig. 8 The 66 mVrms modulation is possible at 250 MHz or even higher, though requiring a higher signal level from the AFG to accommodate the attenuation caused by the interconnect wires and the transceiver resistance.

Summary

High-speed technology continues to evolve to ever higher frequencies, placing pressure on high-speed interconnects. At much lower frequencies, the impacts are seen in PI. PI challenges are generally more related to the low impedance of the circuitry, while signal integrity (SI) challenges are more related to the higher frequencies. Both the PI and the SI challenges must be met to achieve the system-level performance. This includes the testing aspects as well as general operation. As a result, both SI and PI have interconnect challenges, though the challenges are different. This article illustrates one way test instrument interconnects are evolving to support the latest SI requirements.

REFERENCES

1. S. Sandler, "How To Test PSRR, PSNR, and PSMR for Sensitive Applications, Including Optical Transceivers", *EDI CON 2022*, October 5, 2022.
2. "Ultra-low Impedance (20 micro ohm) Measurement using 2-Port Shunt-Through" – *Picotest*, 2019.
3. S. Sandler, "Cable Shield Resistance Issue in a 2-port Impedance Measurement", *Signal Integrity Journal, Web:* https://www.signalintegrityjournal.com/blogs/15-extreme-measurements/post/2306-cable-shield-resistance-issue-in-a-2-port-impedance-measurement.
4. "How to Measure Ultralow Impedance (100uOhm and lower) PDNs", *EDI CON University*, 2018.
5. Parallel Wire Inductance Calculator, Web, https://www.allaboutcircuits.com/tools/parallel-wire-inductance-calculator/.

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REFLECTIONS

DesignCon Returns to January with New Offerings

Suzanne Deffree
Group Event Director, DesignCon

DesignCon, the premier high-speed communications and system design conference returns to its home at the Santa Clara Convention Center in Santa Clara, Calif., with technical paper sessions, tutorials, industry panels, product demos, and exhibits January 31-February 2, 2023.

Education Highlights

DesignCon's conference program covers all aspects of electronic design, including signal integrity (SI) power integrity (PI), high-speed link design, and machine learning.

DesignCon attendee interests have moved back to optimizing high-speed link design, which had been surpassed in recent years by sessions covering SI and PI topics at the die, chiplet, interposer, packaging, and system interface levels, as well as on sessions covering power integrity, distribution, and management.

Below are some of the highest-rated sessions by DesignCon's Technical Program Committee peer reviewers for the upcoming 2023 event:

Strobed or not? A Deep Dive into the Secrets of High Bandwidth 3D Chiplet Interconnect Signaling Design with authors and speakers from AMD. Chiplets are gaining momentum these days and this paper should be very useful for parallel bus and serial link designers and promises to include info on DQS alignment, which is not discussed commonly though it is an important part of the channel performance.

The Influence of EM Field Solver Numerical Solution Space on Measurement Correlation to 50 GHz & Beyond with authors

and speakers from Wild River Technology and Cadence Design Systems. This session delves into understanding the impact of boundary conditions on simulations and is useful when interpreting simulation results. This is an important topic that is not often covered.

3D Connection Artifacts in PDN Measurements is a joint effort from engineers at Amazon Project Kuiper, Ampere Computing, Cadence, Oracle, Samtec, and STMicroelectronics and demonstrates a very practical measurement technique struggled with by many engineers.

Managing Differential Via Crosstalk & Ground Via Placement for 40+ Gbps Signaling, presented by engineers from GigaTest Labs, MathWorks, SiGuys, and Xconn Technologies, promises to provide a very useful analysis framework that is transferable to other topologies.

Comprehensive Statistical Analysis of SERDES Links Considering DFE Error Propagation from Ericsson and Siemens EDA engineers. This paper proposes a new methodology to analyze DFE error propagation. The technique should improve simulation accuracy for SerDes links without significantly increasing computation time.

Tutorial – Design & Verification for High-Speed I/Os at 10 to 112 & 224 Gbps with Jitter, Signal Integrity, & Power Optimized presented by engineers from Intel will review the latest design and verification developments, as well as architecture, circuit, and deep submicron process technology advancements for high-speed links.

Panel – The Case of the Closing Eyes: Bridging FEC to Signal Integrity with a lineup of experts from Anritsu, BitifEye, Broadcom, Intel, Keysight, Marvell, and Tektronix will provide a lively debate on the role FEC plays and how it can be impacted by signal integrity challenges and what to do with a testing architecture designed to help find a bridge between FEC and SI.

Panel – PCI Express Specification: A High-Bandwidth, Low-Latency Interface for the Compute Continuum includes speakers from AMD and Intel and provides a technical overview of PCIe 6.0 architecture, a preview of the PCIe 7.0 specification features and benefits, and what's to come for PCIe technology.

Event Passes & Additional Information

The 2023 event pass will provide more options and more ways to connect with the educational offerings of DesignCon than previous years.

Ahead of the event, DesignCon will offer five webinars on its digital platform for those registered for the Santa Clara, Calif., event. These webinars, as well as select sessions recorded at the 2023 event, will be available for review online through February.

Conference passholders will continue to have access to the 14 tracks of education, with more than 100 sessions curated by our 97-person Technical Program Committee. All DesignCon attendees will have access to sessions focused on emerging chips and markets, presented by IEEE Spectrum, at our 2023 event. Additionally, for the third year, DesignCon also adds the Drive World conference as a complimentary track for All-Access and 2-Day passholders, where conference attendees will have access to technical education on automotive electronics and intelligence. In total, DesignCon is offering more than 115 educational sessions.

DesignCon has also added additional networking options for 2023 to complement its popular social events; the Welcome Reception and Booth Bar Crawls. For the first time, DesignCon will present an Emerging Engineer breakfast, aiming to offer connections and support to those engineers with less than 10 years of professional experience. The breakfast will coordinate with educational sessions specifically planned to support engineers emerging in their careers.

Additionally, all attendees have access to daily keynotes, panels, Chiphead Theater presentations, exhibitor-led education, the Engineer of the Year and Best Paper Awards presentations, and the DesignCon expo floor.

Among 120+ exhibitors, DesignCon's expo floor will present some of the industry's most influential companies, including host sponsor Amphenol, Cadence, Keysight, Molex, Mouser, Samtec, TE Connectivity, and more. Experts from these companies will be on-site to answer design questions, provide advice on engineering, and present educational demonstrations on the latest in high-speed design tools, technologies, and developments.

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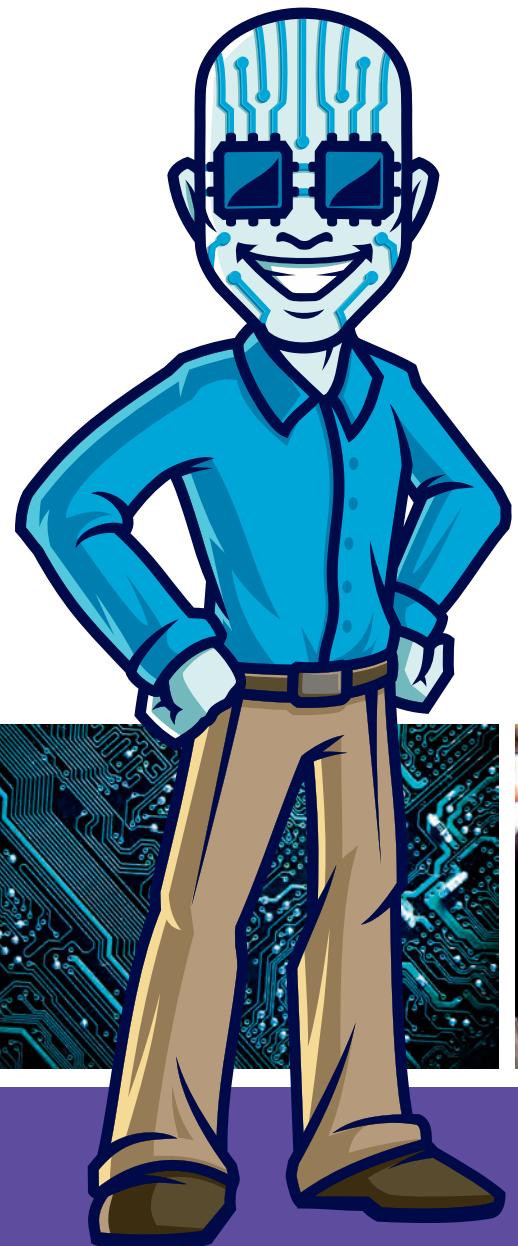

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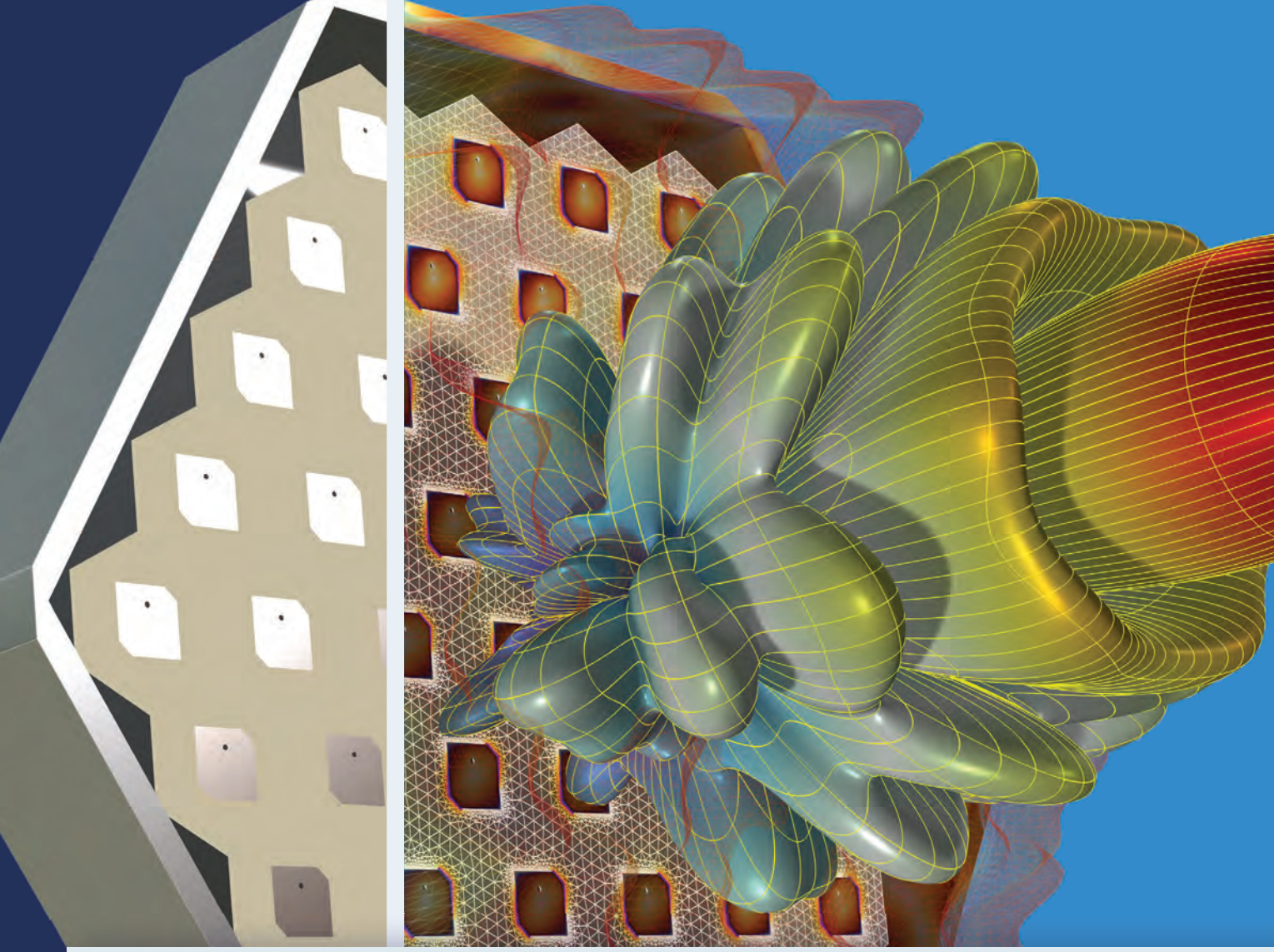

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