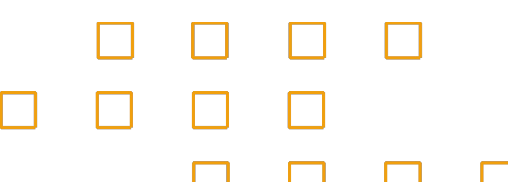

Applications of Semi-Additive Process Technology to PCB Design and Production

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THREE QUESTIONS

1. Are there benefits to shrinking circuits on Printed Circuit Boards?
2. Can you give an example?
3. What are the effects?

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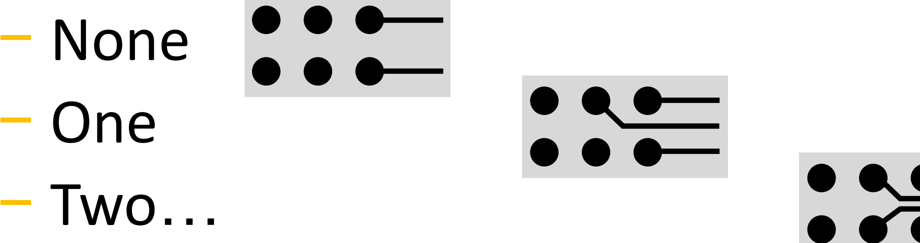
Shrinking Circuits: Where Do We Start?

- What challenges face every layout specialist?
  - Ball Grid Arrays (BGA), routing traces outside of BGA, joining both, etc.
- Which process to use?: Semi-Additive Process (SAP) vs. Subtractive Etch (SE) Process
- General design: look at # of signal lines passing between BGA pads
  - None
  - One
  - Two…
  - Many



- Specific case: circuit layout example
- Look at some electrical effects of shrinking circuits

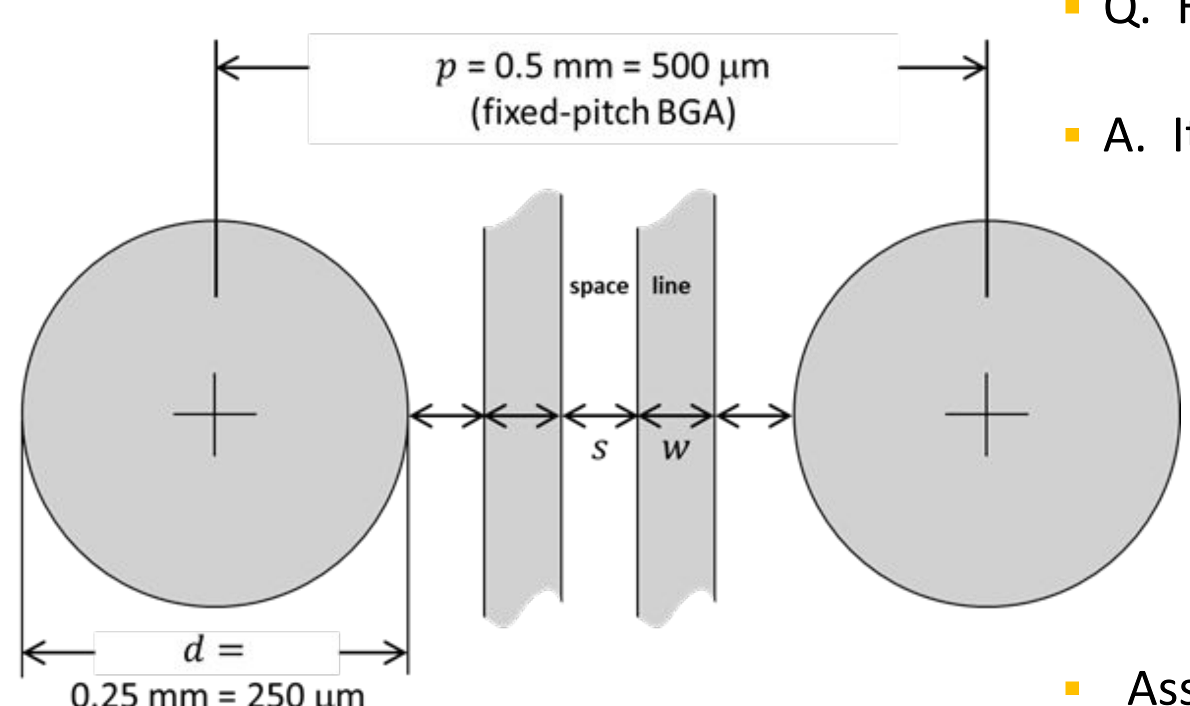
LOOK FOR THESE ON NEXT SLIDES:

- Increase # of traces through BGA

- Reduce # of:
  - layers in PCB
  - laminations
  - microvias

- Combined, these promote:
  - decreased board size
  - higher reliability
  - lower costs
  - smaller environmental footprint

General Case: Ball Grid Array (BGA) Land Pattern



- Q. How many Lines can fit between two BGA Pads?
- A. It depends on the Line width. First, define:
  - p = distance between pad centerlines (pitch)
  - d = diameter of pads
  - w = width of metal line(s)
  - s = width of space(s) between adjacent metal
  - m = the number of possible equal spaces
  - n = the number of possible equal lines
- Assume:
  1. All pads are for signals (worst case for routing)
  2. Line width = space between lines

Calculating the number of Lines, n

- $m = n + 1$ [Eq. 1]
- $p = d/2 + (m*s) + (n*w) + d/2$ [Eq. 2]
- $n = \text{Int}[(p - d - s) / (w + s)]$ [Eq. 3]

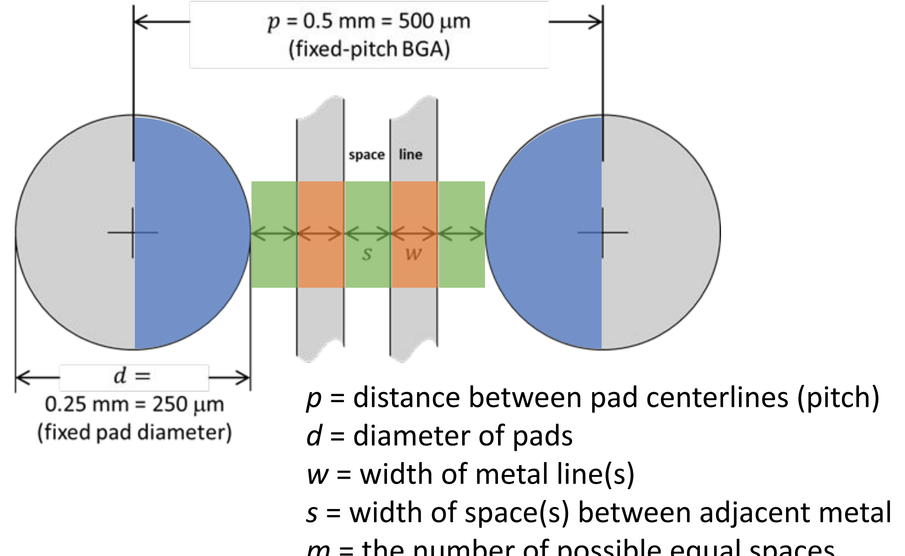


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Table of "n" for Different Minimum Feature Sizes

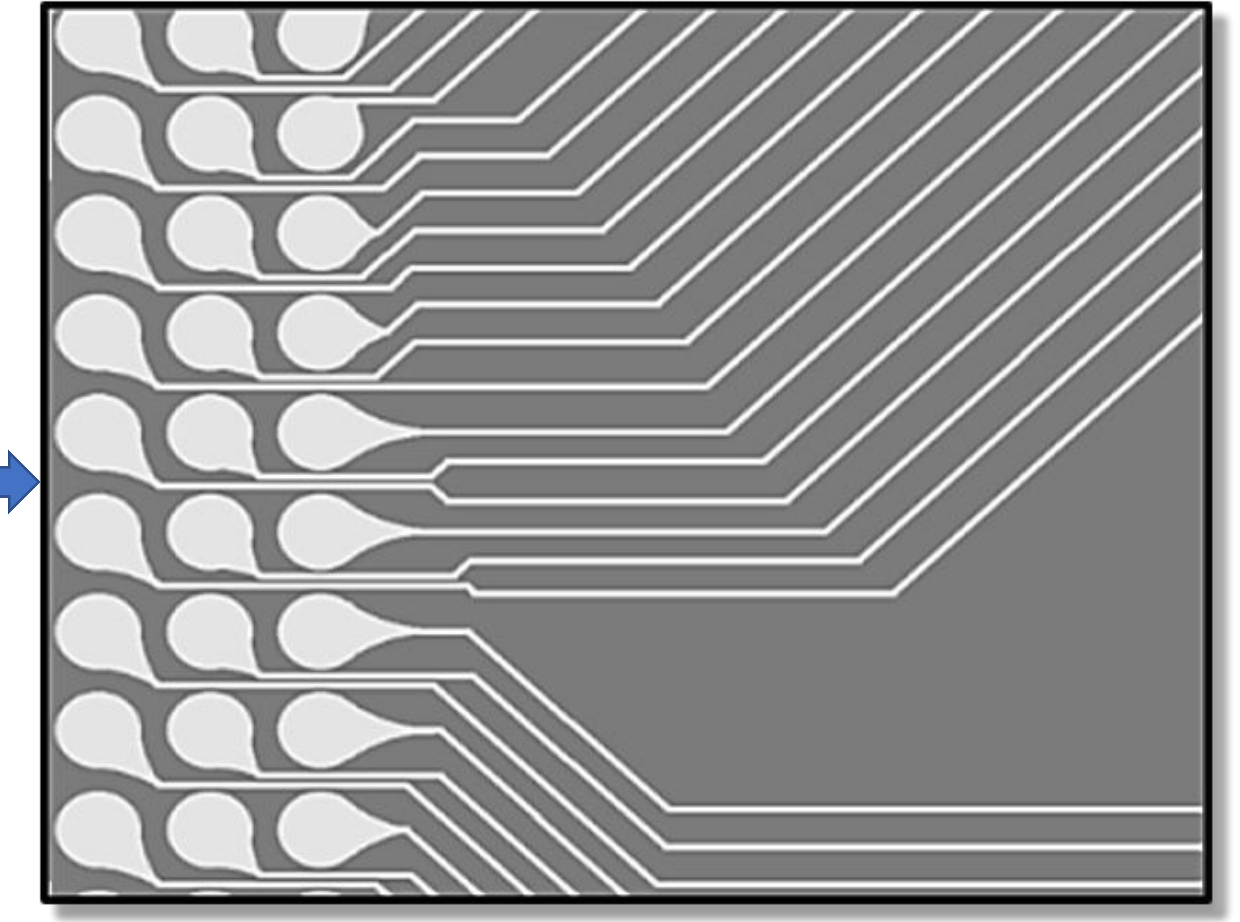
Ball Pitch	Line & Space (minimum feature size, s and w)	Routing Layers Required	# of Lines (between pads, n)
0.5 mm	75 µm	12*	1
	50µm	6	2
	35µm	4	3
	28µm	3	4
	19µm	2	6
	10µm	1	12

SE
SAP

Notes:
1) * = starting assumption
2) ∴ [R.L.R. ∗ (# Lines)] = constant; 12 in this example
3) white rows – see next pages

BGA Land Pattern, 50x50 BGA Grid, 100 μm-Line Pitch

Ball Pitch	Trace & Space (minimum feature size, s and w)	Routing Layers Required	# of Traces (between pads, n)
0.5 mm	75 μm	12	1
	50μm	6	2
	35μm	4	3
	28μm	3	4
	19μm	2	6
	10μm	1	12



BGA Land Pattern, 50x50 BGA Grid, 38 µm-Line Pitch

Ball Pitch	Trace & Space (minimum feature size, s and w)	Routing Layers Required	# of Traces (between pads, n)
0.5 mm	75 µm	12	1
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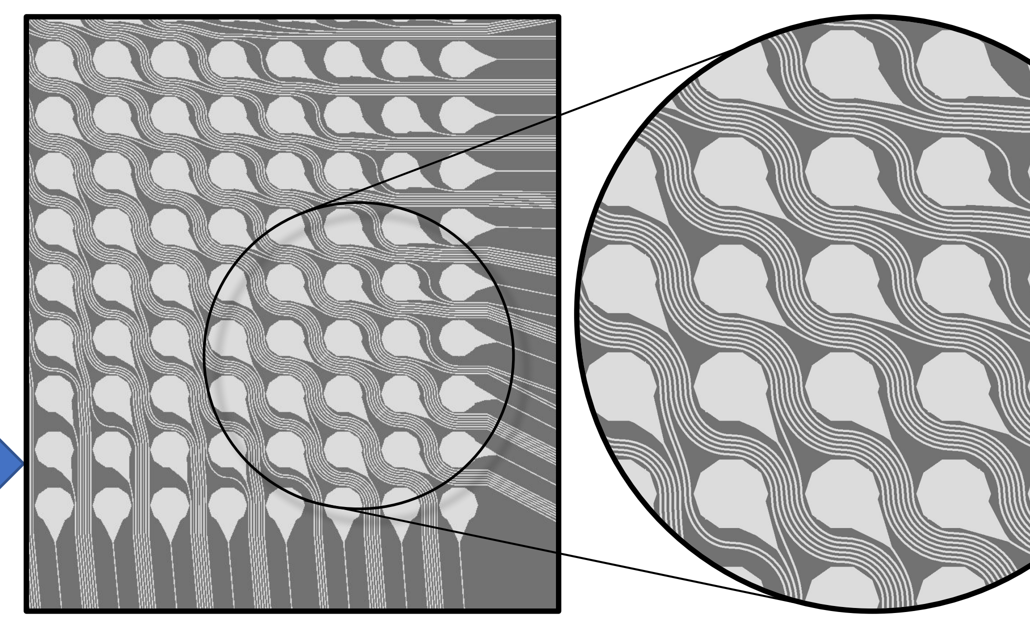

Routing More Lines Between Pads

By decreasing linewidths:

- Can route more traces through a BGA
- This reduces the # of routing layers
- Compare SAP and SE for
  # of lines between pads
  - SE upper limit is about 1 trace
  - SAP upper limit: photolithography limited

Benefits of using SAP Technology in PCB Designs

- Increase # of traces through BGA
- Reduce # of:
  - layers in PCB
  - laminations
  - microvias
- Combined, these promote:
  - decreased board size
  - higher reliability
  - lower costs
  - smaller environmental footprint

- Can design with much:
  - shorter line lengths
  - thinner dielectrics
  - thicker dielectrics (& use tightly-coupled differential conductor pairs)
- Could combine low-density SE layers with high-density SAP layers in one board design

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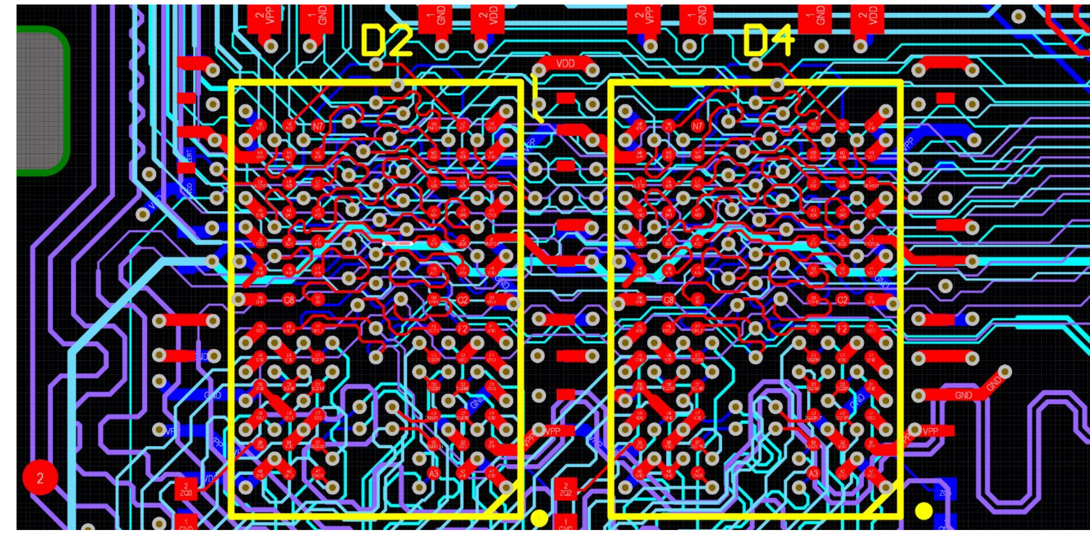
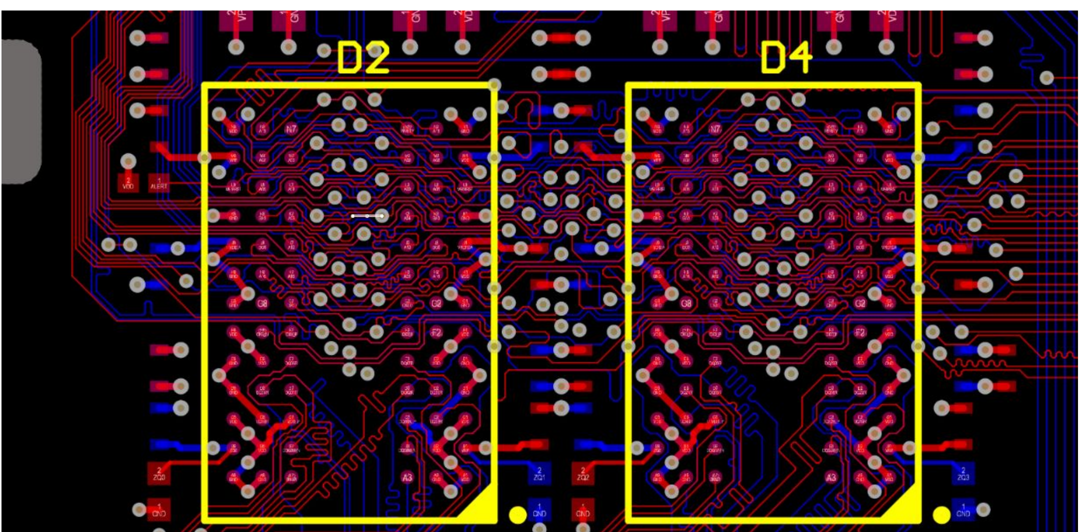
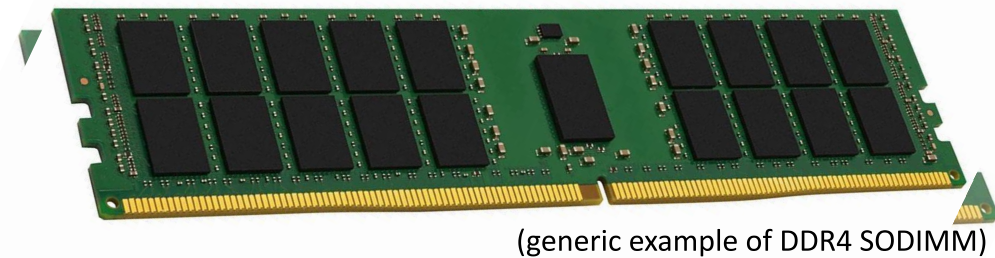
Specific Circuit Application Example: DDR4 S







(generic example of DDR4 SODIMM)

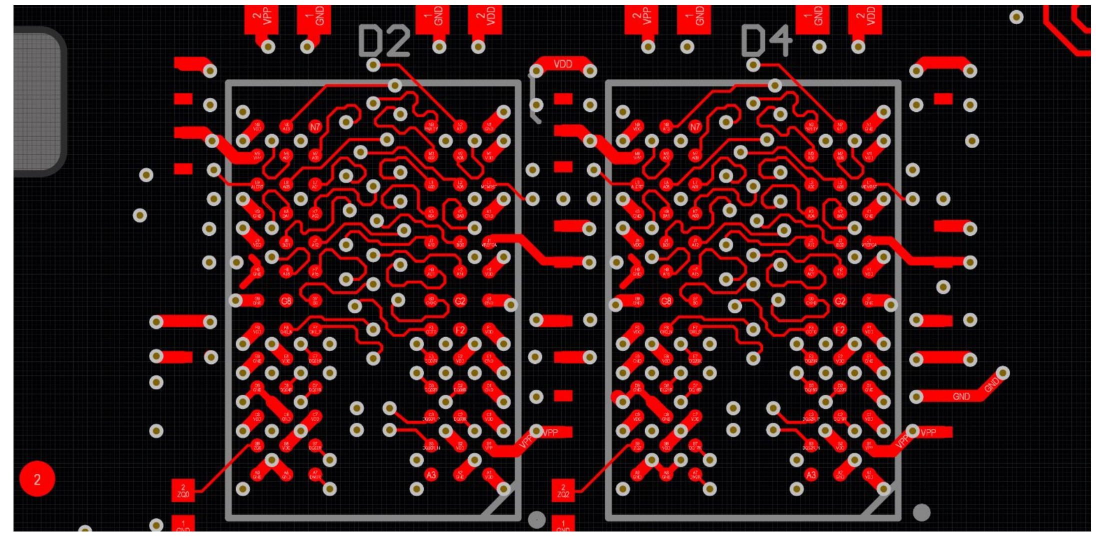
- DDR4 SODIMM reference design (above)
- Multi-layer CAD drawings (at left)
- *Upper drawing*: original reference design, 75 um lines and spaces for SE Process
- *Lower drawing*: re-design, using SAP design guidelines, 35 um line & 52.5 um space

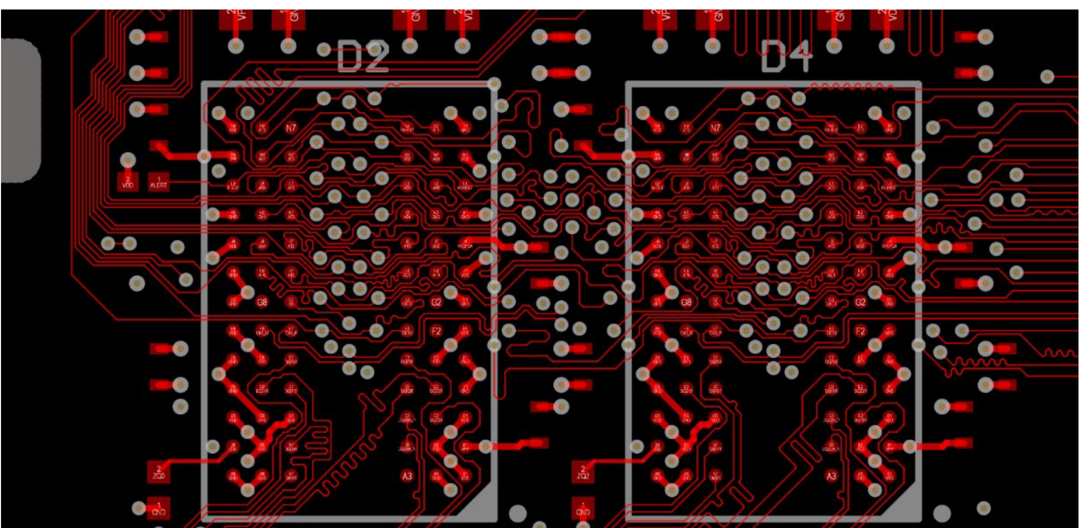
(Courtesy, T. Chester, Ref. [3] & Altium)

Notes:

(1) SODIMM (or SO-DIMM): Small Outline Dual In-Line Memory Module
(2) DDR4: Double Data Rate 4
(3) e.g., https://resources.altium.com/p/fly-topology-routing-ddr3-and-ddr4-memory

Specific Example: DDR4 SODIMM (cont'd.)





- Same circuit
- Focus: Signal Layer around BGA land pattern, single metal layer views
- *Upper drawing*: original design 75 um lines and spaces for SE. One or two lines fit.
- *Lower drawing*: SAP version of the same circuit. Up to four lines run between pads.

(Courtesy, T. Chester, Ref. [3] & Altium)

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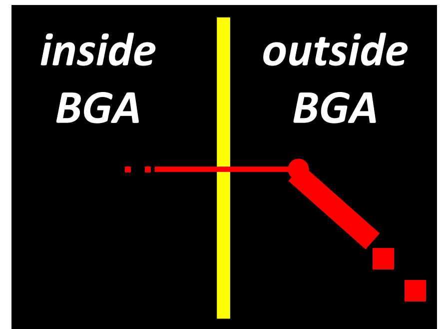
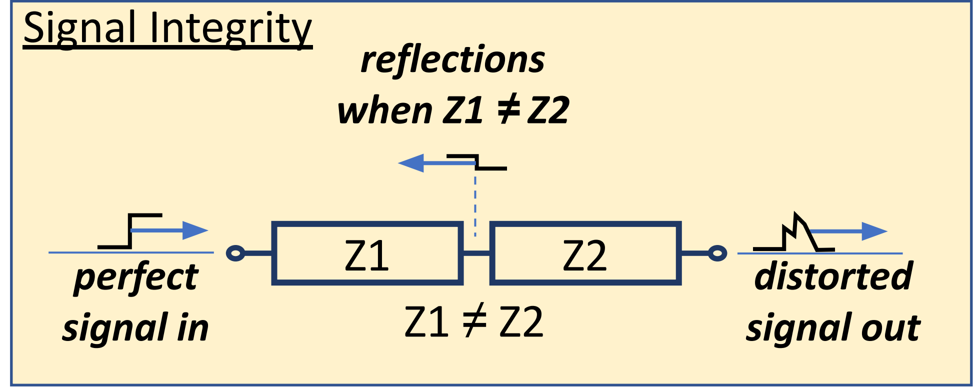
Considerations





- Look at joining finer lines at the BGA to wider lines outside
- Board designs typically use a Characteristic Impedance of Z_0 = 50 Ohm for signal lines
- However, when signals meet mismatched impedances, reflections result & can distort the signal
- Signal Integrity (SI): potential signal distortion = ***f*(**impedance, line length, slew rate, etc.**)**

Refs. [5 – 7]

Impedance Variation

- Q1. Why Z_0 = 50 Ohms?
- Q2. Where does $Z_0 \neq$ 50 Ohms?
- Q3. Why?
- Q4. When does it matter?
- Q5. How much?

A1. This is a practical but arbitrarily-chosen standard value. Often, Integrated Circuit I/O's are designed to it.

A2. Generally, where a metal line cross-section changes*

A3. By (i) design or (ii) through manufacturing process variation

A4. When good Signal Integrity (SI) becomes critical

A5. Today, +/- 10% Z_0 tolerance is accepted. Too often, it can't be achieved. Moreover, we see this spec tightening into the future.

Note: * – other factors also apply. See, e.g. Refs. [5 – 6]

Two Sources of Impedance Variations due to Widths

- Manufacturing Process Variations in width
  - From process variation: across a panel, within a batch, batch-to-batch, etc.
  - Impedance (Z_0) change: Z_0 ↑ as line width ↓ (see next slide)
  - Possible Signal Integrity (SI) degradation if I.C.'s Z_0 not matched to line's Z_0
  - However, there is less process variation with SAP compared to SE

- Intentional Design Changes in width
  - Uneven-size metal lines joined by design (e.g. route lines away from BGA)
  - Signal reflections may occur any time there is impedance mismatch
  - Reflection magnitude depends on many factors
    - Q. Are the reflections significant?
    - A. Must do SI analysis (line length, signal slew rate, etc.)

Impedance Changes from Process Variations

EXAMPLE: DIELECTRIC
THICKNESS ≈ 5 mils (127 µm)
Dk = 4.0

METAL TRACE
WIDTH ≈ 10 mils (254 µm)

SAP variance
Tight impedance control with SAP will even benefit wide lines (10 mil nom)

Typical SE variance
$Z_0 \approx 50$ +/- 5 [Ω]
= nom +/- 10 %

$Z_0 \approx 50.2$ +/- 0.25 [Ω]
= nom +/- 0.5 %

□ *getting narrower* || *getting wider* □

CHARACTERISTIC IMPEDANCE, Z_0 [Ω]: 55.0, 54.0, 53.0, 52.0, 51.0, 50.0, 49.0, 48.0, 47.0, 46.0, 45.0

-30, -20, -10, 0, 10, 20, 30

DEVIATION, ACTUAL WIDTH vs. NOMINAL DESIGN LINE WIDTH [microns, µm]

- Microstrip transmission line
- Assume:

  - one 10 mil-wide trace (250 um)
  - 5 mil-thick dielectric
  - Dk = 4.0
  - ground plane beneath
- Variations:
  Processing □ Width
- Calculate the impedance, Z_0, as line width changes

[7]

Effects of Line Width Changes (cont'd.)

- Tighter manufacturing tolerance on linewidth with SAP gives tighter Z_0 than with SE
- Intentional width changes by design, such as during PCB layout (e.g., routing out of BGA)
  - Even more dramatic DZ_0 , compared to manufacturing process
- Impedance changes will result in reflections. The lengths of the lines also play a role
- Therefore, signal integrity must consider both effects

  (i) design

  (ii) process

Conclusions

- We've demonstrated a SAP PCB layout on the signal layer of a DDR4 SODIMM circuit

- SAP
  - minimizes line widths and their processing variations
    - allows more lines between BGA for many benefits
    - fewer layers, laminations, and microvias
    - …resulting in lower production costs and higher reliability
    - worth pursuing, especially for designs with large BGA pad counts
  - SAP layers may be combined with SE layers in the same board

- Proper routing requires careful considerations of signal integrity

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- Tomas Chester/Chester Electronic Design: DDR4 SODIMM re-design using SAP
- Eric Bogatin and students / CU Boulder: signal integrity

Please Look for This Upcoming Paper

E. Bogatin, C. Suresh, M. Piket-May, Univ. of Colorado,

and H. Basit, P. Dennig, Averatek Corp., "Utilizing Fine Line PCBs with High Density BGAs,"

Signal Integrity Journal [manuscript submitted for publication]. To be available:

https://www.signalintegrityjournal.com

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