A Review of Additive Electronics

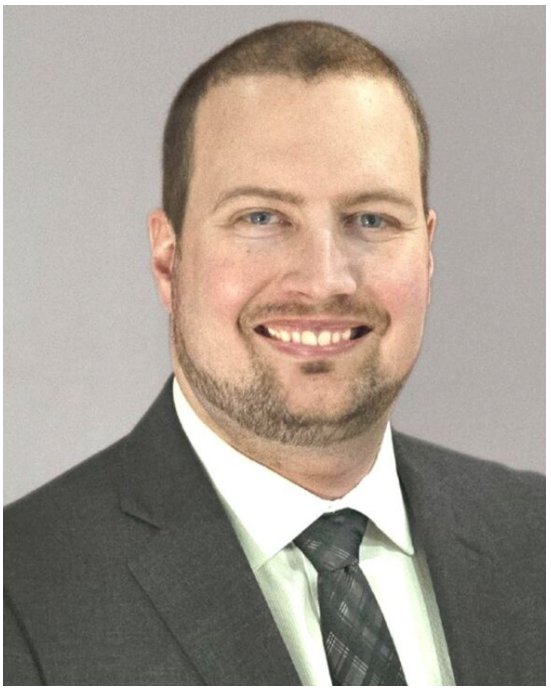
Additive electronics for PCB fabrication is in the spotlight for the capacity to form much tighter feature sizes than typically available from subtractive-etch processes (SAP), with significant RF benefits. This is opening new possibilities for PCB designers as they navigate the increasingly complex balance between functionality, size, and complexity. As with any new technology, there is a learning cuve. This is the second in a series of columns intended to shed light on the experience these early adopters have gained. Today, I am speaking with Tomas Chester, Founder and hardware designer for Chester Electronic Design.

Tomas, you are a well-known designer and instructor, but for those who have not had the opportunity to meet you, could you please start with a quick introduction?

I am a Hardware Design Engineer from Ontario, Canada. In 2017 I founded my own contracting and consulting firm Chester Electronic Design. Since then, I have worked on all manner of boards, from IMS to Semi-Flex. In 2020 I started the Ontario Canada PCEA Chapter and in 2021 I joined the PCEA Executive board. I am also a full time Altium Instructor teacher their *Essentials* and *Advanced* courses.

That is an impressive resume! Founding your own contracting and consulting firm requires familiarity with many different types of technology. One thing you and I have talked about quite a bit: potential benefits of using 25 micron trace and space or below in PCB design. What were some of your first thoughts - what caught your eye?

I initially jumped to the possible uses in those ultra-small design cases. I can see a lot of uses for technology like this: in the medical space, or even in wearable devices. Being able to have such small traces is goin to enable not only smaller designs, but *higher utilization of existing space* - which will lead to the reduction of raw materials required to build a design.



TOMAS CHESTER

Founder & Hardware Designer for Chester Electronic Design

You had a few questions early in our discussion that are going to be common for PCB designers...

1.What trace gap distance is possible?

With the right photolithography set-up, as small as 12.5 microns has been tun. Most fabricators can do 20 to 25 microns.

2. As this is an additive process, how tall of a trace can you get?

Currently, for a 25-microns (1 mil) line a 20 to 25 microns (0.8 to 1 mils) thick line is std with 50 microns (2 mils) possible but not tested. On a 50-microns line a 50-micron thickness can be done.

3. How tight is the line-width control?

Very tight, typically +/- 1 micron (+/- .025 mils)

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4. Do you need to use a special Solder Mask when using a very fine pitch semi-additive design process?

No. Typically the design will end up with an LCI-imageable mark, but that is very common now. Consideration needs to be given to mask-defined pads over copper defined to keep the adjacent traces covered.

5. Where in the design fabrication process does this fit?

The semi-additive process (SAP) is completed early in the fabrication process. To over-simplify: where traditional subtractive-etch processes start with a copper clad laminate panel and etch away the copper that is not required, the semi-additive approach begins with the base dielectric - and adds copper to the panel only in selected areas.

6. Can you mechanically drill with SAP, or do you need to use a special drilling process?

Both mechanical drill and laser drill can be used with semi-additive process

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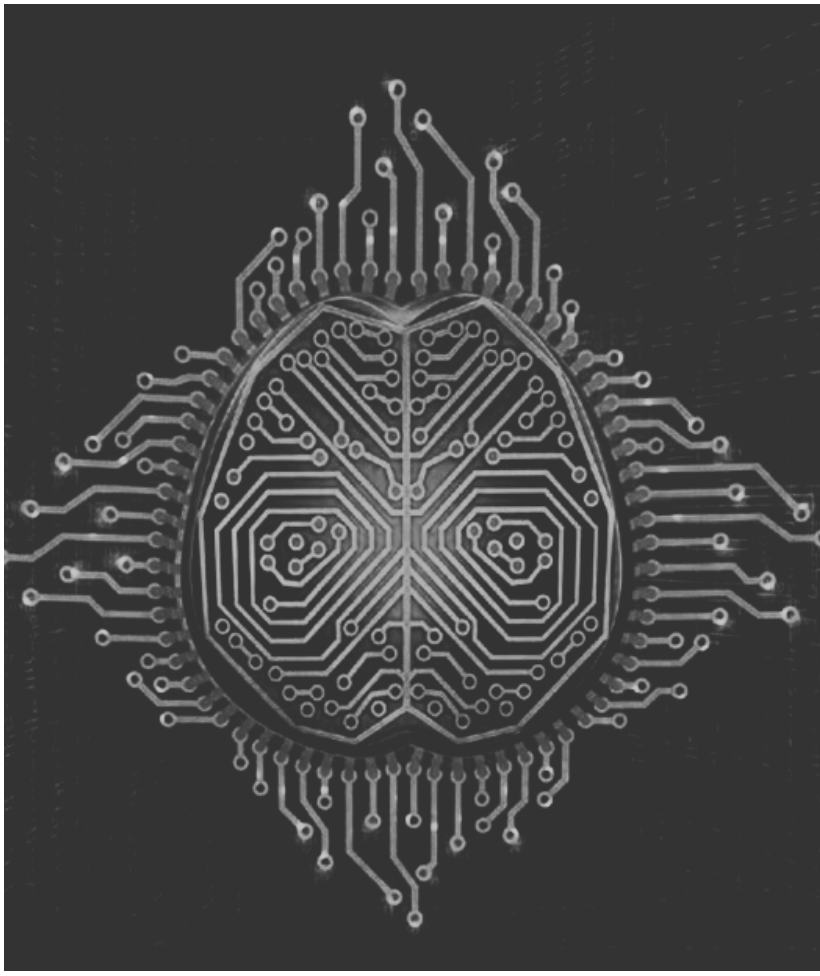
We are just scratching the surface on how best to apply these new fabrication capabilities to PCB design. There are obvious benefits to overall size and weight. There is also the potential to reduce layer count, lamination cycles and the number of microvia layers needed, which all increase yield and overall reliability. What aspect of these new PCB fabrication capabilities is most valuable to you?

All designers are going to be excited about the ability to access these benefits. Personally, I am excited about the ability to break out of µBGA part without needing to do other HDI design strategies.

You are currently working on a project that is redesigning an Altium reference design, applying a 25 micron trace/space where it makes sense. Can you tell us a little about the project?

To get a better understanding of some of the requirements and difficulties associated with designing a SAP product, I am working on using an existing Altium DDR4 SODIMM design to reimagine it - utilizing SAP. This is resulting in some promising improvements with respect to layer reduction, and it also has reduced the overall complexity of designing a DDR4 Fly-by architecture.



As with any Engineering process, there are some assumptions that have been made with respect to the design as we are still in the early days of SAP, so this is intended as a learned and educational piece - with an understanding that it may not be functional.

However, it is more about the experience and getting that key information on how to implement SAP into a design and what improvements come out of it. The key is this situation is having an existing design that we can refer back to and compare the changes once we complete the design.

I am looking forward to those results. Working with something new can be exciting and just a little intimidating - navigating the learning curve, do you see any challenges for designing with this new technology in mind?

I think that there are some challenges that will need to be overcome. Due to the changes in trace size - and also with respect to how new this process is - the Impedance and the Field Theory around using this in a design is still being developed. The SAP process means we are shifting away from planar coupling of traces, and starting to deal with broadside coupling and the requirements for co-planar wave guides. Currently, there is no proper way to calculate what this is going to do at such a small scale, which could cause all sorts of design and signal integrity issues.

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Get in touch with your fabricator as early as possible and make sure you discuss this with them

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Tomas, what advice would you give to PCB designers who are just hearing about the opportunity to work with fabricators that can now offer these fine feature sizes?

Get in touch with your fabricator as early as possible and make sure you discuss this with them. They will have all kinds of insight on what to do, and having them review your design as you progress will increase the chances of a Revision A success. They will also be able to give you additional details about their capabilities, and any issue areas they have encountered on other previous designs.

Thank you so much for talking with me today. If people want to get in touch with you to learn more, what is the best way to reach you?

Best way to get in touch is on my website or my email. Thank you.

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