

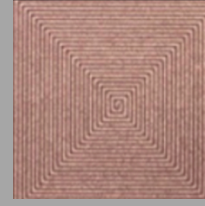
Pin-Out Challenge: Rethink the Solution



Capability in USA Today
75 microns



mSAP Capability Today
25 microns



AVERATEK Capability Today
15 microns or better

PCB Talk

Semi-Additive PCB fabrication is getting a lot of attention, as it enables fabricators to provide much finer features than traditional subtractive-etch processes. **The revolutionary Averatek Semi-Additive Process (A-SAP™) package and interconnect solution can reduce size and weight by 90% over traditional processing techniques in the U.S., with 25 micron space/trace features and significant signal integrity benefits.** This is opening new opportunities for PCB designers to solve complex challenges.

With any new technology, there are many questions: how to apply this capability in design, optimize its advantages, and how to work with the select fabricators who offer it.

Thought leaders in Design are enthusiastic about navigating this new frontier

Cherie Litson, MIT CID/CID+ is a recognized design expert: President of her own consulting firm, a Master Instructor for the IPC Designer Certification Litson1 Consulting, and an Instructor at Everett Community College.

With a background that is broad and deep, her experience includes creating the wireless mouse for Microsoft and the design database for Surface, and the first hand-held ultrasound for SonoSite.

She is passionate about PCB design - and about golf. Cherie has been involved in the LPGA Amateur Association (previously EWGA) since 2001, and has taken her teams from to national competitions for the past five years. Let's tee up this discussion!



CHERIE LITSON, MIT CID/CID+

Master Instructor - Design

What aspect of these new PCB fabrication capabilities is most valuable to you?

I am excited by the ability to route traces at 1 mil or even below, as that opens up possibilities for designers to produce increased density at lower cost. The A-SAP™ process provides the designer an opportunity to significantly reduce layer count, simplifying complex designs.

Designers working on next-generation products will be excited about the ability to form a 15µm trace and space with the semi-additive processes. Many designs are being driven to require line and spaces at 50µm due to smaller pin spacing on components and smaller package products. The fabrication of these traces is something that has not been available in the US until now.

Averatek



TARA DUNN

VP Marketing &
Business Development,
Averatek Corporation

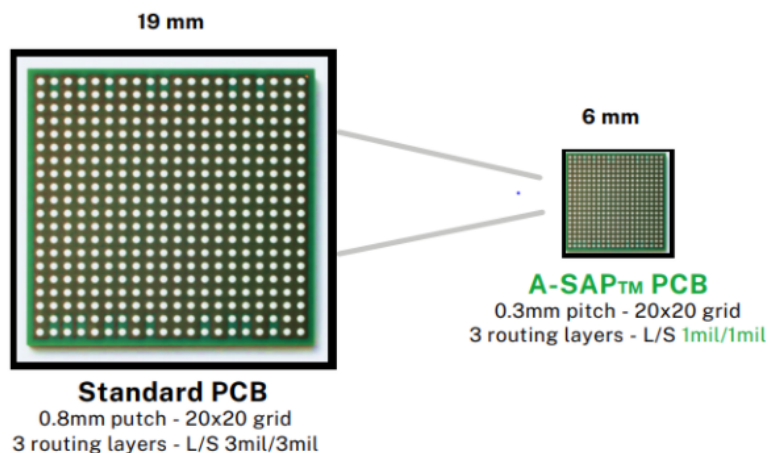
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"These geometries can potentially eliminate pin out challenges while maintaining reliable signal integrity. I can see the advantages of using a taller yet narrower trace for signal integrity - that is the winning factor for me. This process results in traces with horizontal rather than trapezoidal sidewalls, realizing benefits in both size and RF advantages, eliminating the etch comp requirements."

You are an avid learner - when you are researching new technology, which reliability tests mean the most to you?

As I consider how to best apply this technology, material compatibility is an important aspect. It is important to know that a new process is going to be compatible with nearly all materials. Next, I'm looking into the electrical aspects of these new geometries.

I also look at proven reliability parameters: the process passed peel strength, IST coupon testing, and signal integrity analysis across a variety of materials.



Working with something new can be exciting and just a little challenging; navigating the learning curve, do you see any issues for designing with this new technology in mind?

In my opinion, designers should remember their basic electronics - it influences everything we do. We must understand the physics to make certain we know what will be affected. With these new parameters, we will need to go back and take another look at our calculations, which are based on the resistance of copper - which is based on the area. Then bring into the equations the resistance of the dielectric materials, layer structures, etc. I am curious to see how the geometry of the conductors shifts the electrical results.

Why do you feel that this new technology is important to the industry?

A number of reasons: implementation of this process - it is designed to integrate with existing PCB fabrication equipment, so **it does not require the costly capital investment** usually associated with new technologies, allowing even the smaller and mid-size shops to offer this advanced technology to their customers.

While the A-SAP™ process gives us the benefit of 25µm line/space and below, the additive process also has RF benefits at larger feature sizes, improving impedance control. I think we are just scratching the surface of how to get the most benefit from this capability. I am already seeing the simplification of complex designs, improving yields, reducing costs. I am excited to see where this technology takes us.



"Averatek, a Silicon Valley innovation company, manufactures key chemistries and licenses the processes for their use. Two processes in particular are having an effect on the PCB Design industry: LMI™, the catalytic ink used in the A-SAP™ process, and Mina™ a surface treatment that enables soldering to aluminum. These products are now commercially available through licensed fabricators, so it is important for designers to learn about them."

Cherie, as we wrap up, what advice would you give to PCB designers who are just hearing about the opportunity to work with fabrication that can now offer these fine feature sizes?

Start today! Do some research, share your concerns, share your experiences, try it out. I can see many benefits to utilizing this process at the 75µm, 50µm, & 25µm trace sizes and smaller. **Averatek is forming a Community of Interest, to bring together a wide range of people from all sectors of the industry that are interested in learning more about semi-additive PCB processes. We are developing a platform to pool our knowledge - stay tuned!**

