Applications of Semi-Additive Process Technology to PCB Design and Production

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Abstract

Traditional Subtractive Etch (SE) processes used to manufacture Printed Circuit Boards (PCBs) are adequate for many of today's circuit designs. However, certain parts of PCBs, and more generally, certain PCBs in their entirety, are reaching the lower limits of signal conductor line widths and spaces. Today, these dimensions are typically 75 μm / 75 μm (3 mils / 3 mils). New Semi-Additive Process (SAP) technologies can reach much smaller pitches, typically 25 μm trace plus 25 μm space (1 mil / 1 mil) and below. Because the design step precedes manufacturing, this paper will explore the unique challenges associated with designing for SAP fabrication and offers a framework for maximizing benefits. In a specific example, new SAP design guidelines have been applied to the layout of a reference design for a DDR4 SODIMM module. Benefits include: (i) narrowing the trace pitch to route more traces through the Ball Grid Array (BGA) patterns, (ii) reducing the number of layers, and (iii) decreasing the number of microvias. These efforts result in lower costs due to decreased board size and a lower layer count with fewer lamination cycles. Moreover, these modifications collectively should achieve higher reliability. The SAP layers may be combined with SE layers to build a single board. We will show examples in the DDR4 memory layout where the two processes can be used. This case study represents a natural first step in the transition to using new SAP technologies in next-generation PCB electronics.

Introduction

We begin with a brief review of the physical layout of signal lines. Specifically, we're interested in determining our options and their consequences as we route the lines away from the integrated circuit mounting region. First, we examine a BGA and calculate the number of signal lines that may run between pads as the lines escape the BGA area to connect to the rest of the PCB's devices. We do not consider vias within the BGA here. For a given ball pad size, pad pitch, and trace/space feature size, we wish to generally determine (i) the number of routing layers and (ii) the number of traces between ball pads. The reader is advised to consult trade specifications, such as the JEDEC standards, for specific information [1].

For this, please refer to Fig. 1. Let's define the following quantities:

p = distance between centerlines of pads (pitch)
d = diameter of pad
w = width of metal line(s) running between two adjacent pads
s = width of space(s) between adjacent metal lines or line-to-pad spacing
m = the number of possible equal spaces between pads
n = the number of possible equal width lines between pads

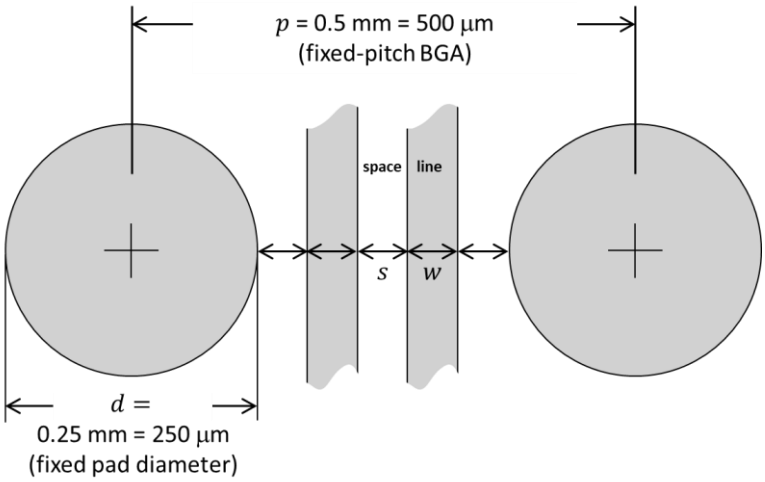


Figure 1 – General Drafting of a Ball Grid Array (BGA) Land Pattern, 500 μm BGA Pitch. The pad-to-pad spacing is fixed in this case at 500 μm center-to-center. That spacing, together with the fixed pad diameter, limits the number of lines and spaces that can fit between the pads. Here, two 50 μm lines fit.

Here, we assume $s = w$. Then, by observing the sample arrangement in Fig. 1, we see that:

$$m = n + 1 \quad \text{[Eq. 1]}$$
$$p = d/2 + (m * s) + (n * w) + d/2 \quad \text{[Eq. 2]}$$

Solving for n, the number of lines, using Eqs. 1 and 2 we find:

$$n = \text{Int}[(p - d - s)/(w + s)] \quad \text{[Eq. 3]}$$

The number of spaces, m, can then be gotten from Eq. 1. We tabulate the results for n, as shown in Table 1, for different minimum feature sizes, s and w. The main point is that we can clearly see the number of routing layers decrease as we add traces between the pads. This results in circuit improvements, such as a decrease in board size, a decrease in the quantity of routing layers, and presumed consequent increase in yield and reliability due to fewer routing layers and laminations. All these factors will result in lower total costs.

Table 1 – Circuit Density Improvement. Note that as the trace and space sizes decrease, the routing layer count is reduced and the number of traces possible between BGA pads increases. The instances representing the two rows in white are illustrated in Figs. 2. It is assumed that the number of routing layers required for the base case of 75 μm line and width is 12 layers.

Ball Pitch	**Trace & Space (minimum feature size, *s* and *w*)**	**Routing Layers Required**	**# of Traces (between pads, *n*)**
0.5 mm	75 μm	12	1
	50μm	6	2
	35μm	4	3
	28μm	3	4
	19μm	2	6
	10μm	1	12

In the above example, we assumed a total of 12 routing layers for the base case of one 75 μm signal line routed between pads. Our scenario here is to assume that all pads join signal lines, for a kind of worst-case routing example. In practice, the number of routing layers would depend on many factors in the board design, including the number of traces that are signal lines versus the number of power and ground lines, where the power and ground lines are located (usually towards the center of the BGA), whether vias are used inside the BGA, etc. Note that the product of the Routing Layers Required and the # of Traces for a given Trace and Space here is a constant, 12.

We now extend these principles to slightly more complete layouts, illustrated in Figs. 2. In those figures, the ball pads are augmented with triangular teardrop transitions to the fine traces that escape the BGA. This intentional addition was made to help minimize mechanical stress risers at the transitions to the metal lines. In Fig. 2a, a general drafting is shown of a Ball Grid Array (BGA) Land Pattern for a 50x50 ball grid, with a 100 μm line pitch. For simplicity, assume all pads are signal pads. This is another example with up to 2 traces between pads as first shown in Fig. 1, with 50 μm trace and space (minimum feature sizes), and 6 quantity required routing layers. In Fig. 2b, we show a general drafting of a Ball Grid Array (BGA) Land Pattern, 50x50 ball grid, 38 μm line pitch. Again, assume all pads are signal pads. This is an example of a similar BGA as shown in Fig. 2a, except here, the finer 19 μm trace and space (minimum feature sizes) easily permit up to 6 traces between pads and use 2 required routing layers. The Fig. 2b inset on the right more clearly shows the details of the drawing to its left.

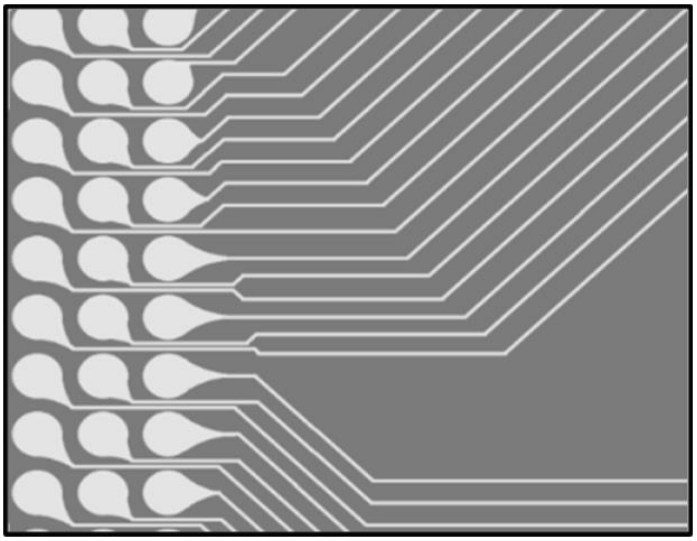


Figure 2a – General Drafting of a Ball Grid Array (BGA) Land Pattern, 50x50 BGA Grid, 100 μm Line Pitch. For simplicity, assume all pads are signal pads. This is another example with up to 2 traces between pads as first shown in Fig. 1, with 50 μm trace and space (minimum feature sizes) and 6 required routing layers. The right-hand side of the BGA is shown.

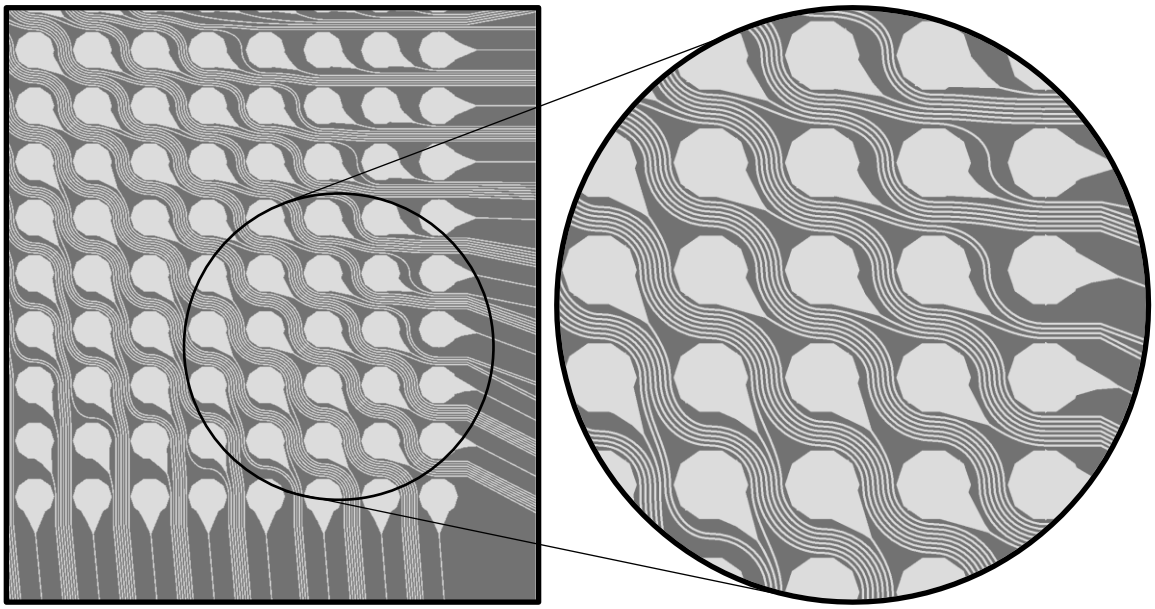
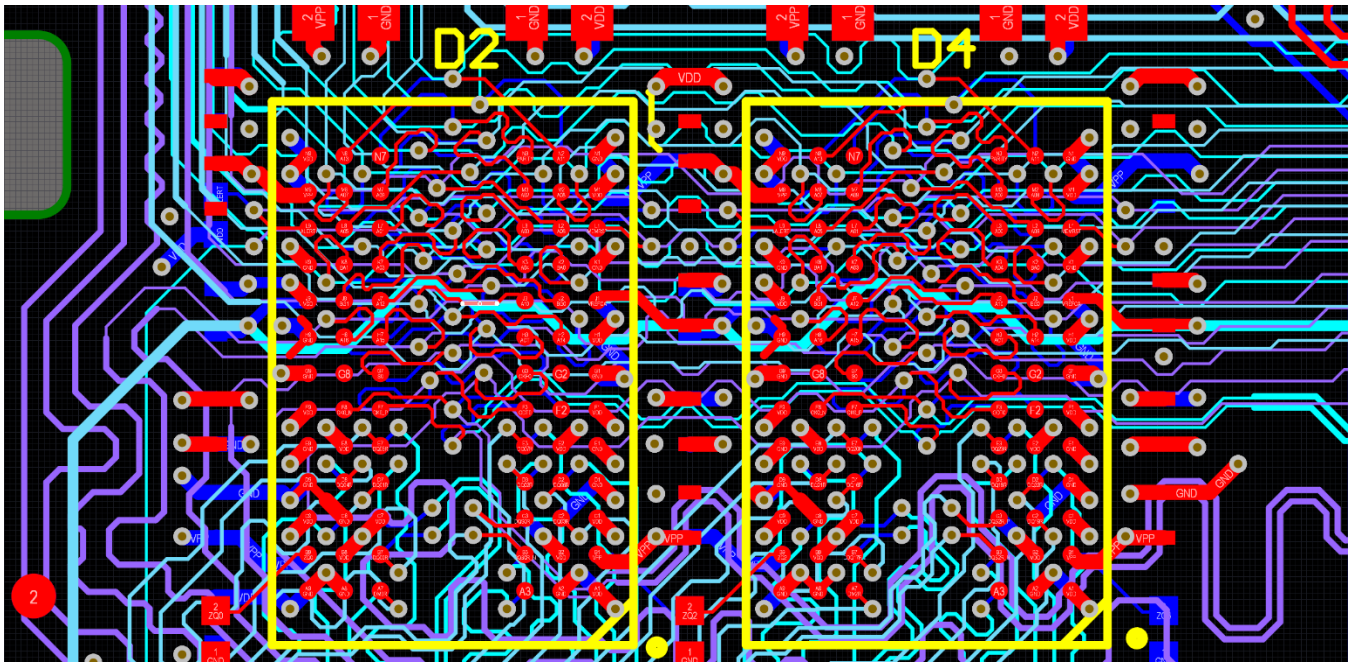


Figure 2b – General Drafting of a Ball Grid Array (BGA) Land Pattern, 50x50 BGA Grid, 38 μm Line Pitch. Again, assume all pads are signal pads. Example of a similar BGA as in Fig. 2a, except here, the finer 19 μm trace and space (minimum feature sizes here) easily permit up to 6 traces between pads and use 2 required routing layers. The inset on the right more clearly shows the details of the drawing on the left. The lower right-hand side of the BGA is shown.

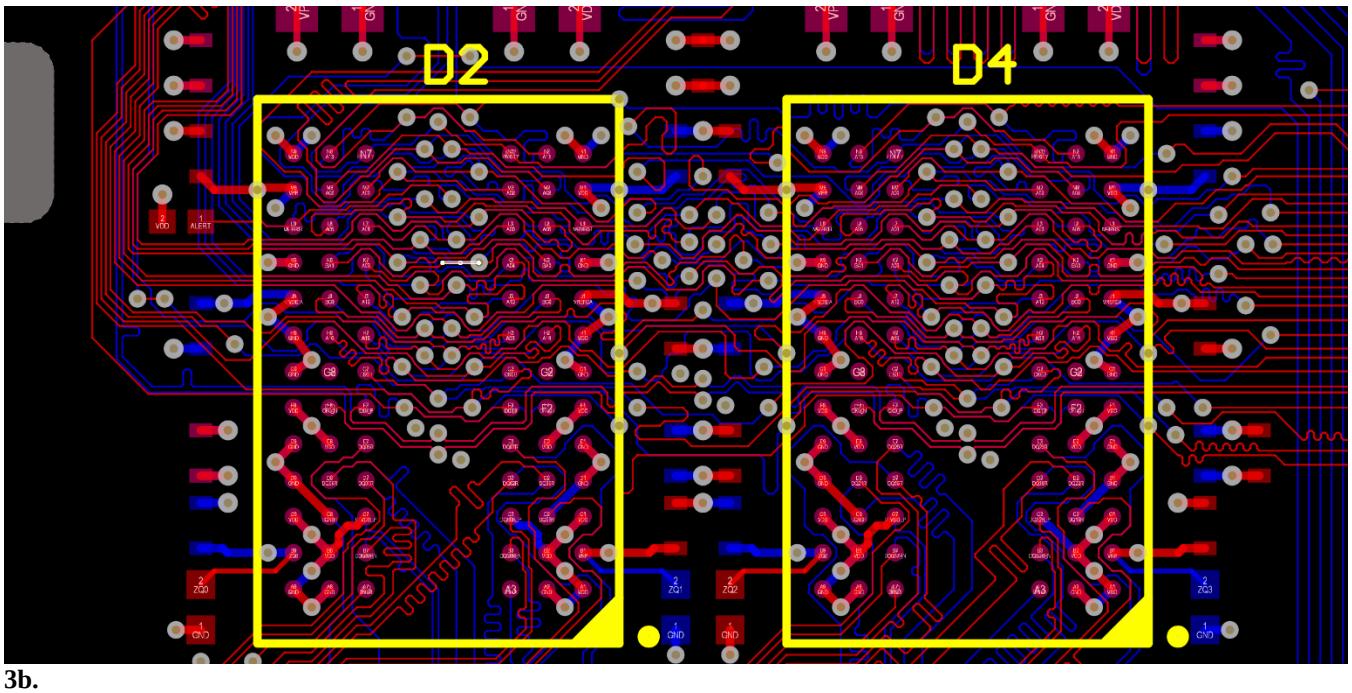
In our Introduction, we have looked at general cases of signal lines escaping from BGA patterns. In practice, standard Subtractive Etch Process (SE) technology may permit only the first row of Table 1, where the minimum trace and space are 75 μm (3 mils) due to process limitations in production.

Specific Example

We now turn to a more advanced topic: moving down the rows in Table 1. We have applied Semi-Additive Process (SAP) design guidelines to the layout of a reference design for a DDR4 Small Outline Dual In-Line Memory Module (SO-DIMM or SODIMM) [2 – 4]. The first results are shown in the multi-layer CAD drawings of Fig. 3.



3a.



3b.

Figure 3. – Signal Layer around a Ball Grid Array (BGA) Land Pattern of a DDR4 SODIMM. The upper drawing, Fig. 3a, shows the original reference design from Altium using 75 μm lines and spaces. The lower drawing, Fig. 3b, is a re-design using Semi-Additive Process design guidelines. (Courtesy, T. Chester [3])

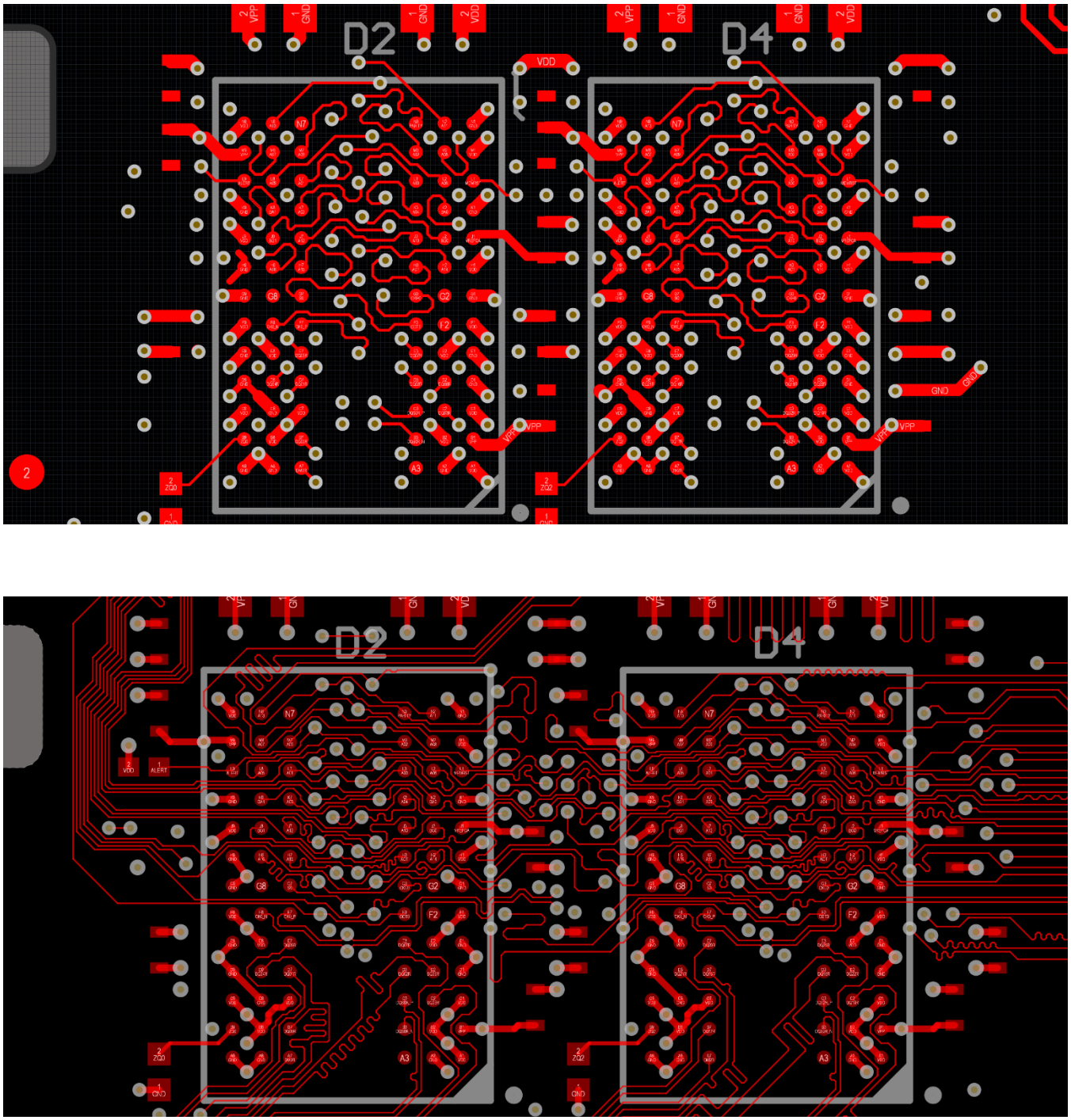


Figure 4. – Signal Layer around a Ball Grid Array (BGA) Land Pattern of a DDR4 SODIMM. These images each show a single layer of signal traces. The upper drawing, Fig. 4a, shows the original reference design from Altium relying on a SE process design rule set using 75 μm lines and spaces, where one or two traces run between pads. The SAP version of the same electronic design using SAP design guidelines is shown in Fig. 4b, where as many as four lines run between pads. (Courtesy, T. Chester [3])

Benefits include: (i) narrowing the trace pitch to weave more traces through the Ball Grid Array (BGA) patterns, (ii) reducing the number of layers, and (iii) decreasing the number of microvias. These efforts result in decreased board size and a lower layer count with fewer lamination cycles. Moreover, these modifications collectively should help achieve higher reliability. All of these factors contribute to lower costs. The SAP layers may be combined with SE layers to build a single board. This case study represents a natural first step in the transition to using new SAP technologies in next-generation PCB electronics.

Discussion

Previously, we have determined options for using finer lines and spaces. However, we have not yet addressed the consequences as we route the fine lines out of the BGA and away from the integrated circuit mounting regions. Board CAD designs typically use 50-Ohm signal lines outside of a BGA pattern. When signals experience mismatched impedances, reflections result. We now need to look at joining finer lines to wider lines beyond the BGAs.

If a digital circuit employs slow slew rates during switching, then the broadband range of electronic signals will likely not suffer too much loss of integrity. However, as switching frequencies and signal slew rates increase with newer circuit technologies, mismatches in impedance at the board level due to joining different conductor geometries play an ever-increasingly important role. Signal integrity may suffer. The lengths of lines, while not affecting the characteristic impedance itself, play a role in determining the magnitude of resulting signals, when forward-travelling waves meet signals reflected from impedance discontinuities.

These are generally the types of considerations that one would cover in RF and microwave engineering, where narrow-band frequency considerations are made [5 – 7]. This is an involved subject beyond the scope of this paper, but we at least introduce some basic considerations here. There are several ways to transmit signals in today's designs. Microstrip, stripline, and coplanar waveguides are but a few choices.

We select a microstrip configuration and choose a specific case as an example. We choose a single 10 mil-wide metal trace, supported on a 5 mil-thick dielectric having a dielectric constant Dk = 4.0. A ground plane beneath this completes the structure. When the metal line is processed, it will be virtually impossible to maintain the width from batch to batch, so we calculate the impedance as the width of the line is slightly varied, to represent line width variation due to process variation. The result is shown in Fig. 5. The impedance was calculated using the microstrip impedance equations in ref. [7]. The point of this example is to illustrate the following two variations in impedance.

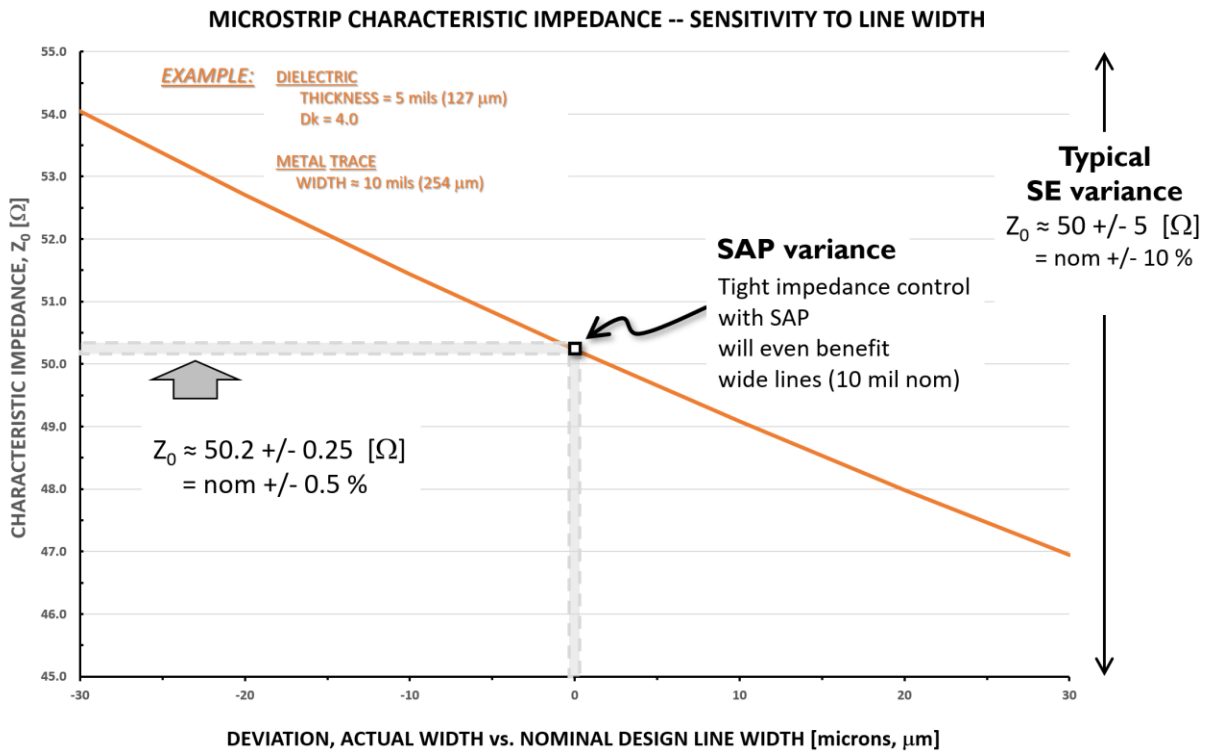


Figure 5 – Impedance Advantage from Line Width Control, SAP Process. Microstrip transmission line example, illustrating that the impedance is controlled to +/- 0.5% tolerance with a Semi-Additive Process, compared to +/- 10% for a Subtractive Etch Process, a better than 10X improvement. This tight line width control from SAP will even benefit the impedance control of wide lines such as the 10 mil-wide shown here.

First, for unintentional changes, even slight variations in width from process variations result in significant changes in impedance. For a Subtractive Etch Process, line width variations are typically specified at +/- 0.5 mils (+/- 12.5 μm), which translates to an impedance spread of +/- 5 Ohms, or +/- 10% of the nominal value. In comparison, for a Semi-Additive Process which can hold a line tolerance of roughly +/- 1 μm, the resulting variation in impedance is within +/- 0.5%. The SAP advantage is easily 10X better than for SE.

Secondly, for intentional width changes, such as when routing metal traces out of the BGA, we can expect even more dramatic changes in impedance resulting from the changes in geometry where lines of different widths join. These will result in reflections. The lengths of the lines can and likely will also play a role in determining the impact on signals. Therefore, for intentional changes in width, detailed considerations of the effects of design on signal integrity are warranted [5 – 6].

Conclusions

Increasing the number of signal paths between the pads of a BGA will decrease production costs, while increasing yield and reliability. To do this requires using an advanced process and design guidelines that can minimize line width variation from processing. Additional changes in line width can intentionally occur when leading signal lines out of a cramped BGA region to other parts of the PCB. Doing that will require careful considerations of the effects of design on signal integrity. We have demonstrated that Semi-Additive Process design guidelines may be used on signal layers of a DDR4 SODIMM layout. These activities have the potential to reduce the board size, total layer count, and number of lamination cycles. They are therefore worth pursuing further for other designs, especially those with large BGA pad counts.

References

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