Applications of Semi-Additive Process Technology to PCB Design and Production

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THREE QUESTIONS

1. Are there benefits to shrinking circuits on Printed Circuit Boards?

2. Can you give an example?

3. What are the effects?
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Shrinking Circuits: Where Do We Start?

- What challenges face every layout specialist?
  - Ball Grid Arrays (BGA), routing traces outside of BGA, joining both, etc.

- Which process to use?: Semi-Additive Process (SAP) vs. Subtractive Etch (SE) Process

- General design: look at # of signal lines passing between BGA pads
  - None
  - One
  - Two…
  - Many

- Specific case: circuit layout example

- Look at some electrical effects of shrinking circuits
Benefits of using SAP Technology in PCB Designs

LOOK FOR THESE ON NEXT SLIDES:

▪ Increase # of traces through BGA

▪ Reduce # of:
  – layers in PCB
  – laminations
  – microvias

▪ Combined, these promote:
  – decreased board size
  – higher reliability
  – lower costs
  – smaller environmental footprint
Q. How many Lines can fit between two BGA Pads?

A. It depends on the Line width. First, define:

- $p$ = distance between pad centerlines (pitch)
- $d$ = diameter of pads
- $w$ = width of metal line(s)
- $s$ = width of space(s) between adjacent metal
- $m = $ the number of possible equal spaces
- $n = $ the number of possible equal lines

Assume:

1. All pads are for signals (worst case for routing)
2. Line width = space between lines
Calculating the number of Lines, n

- \( m = n + 1 \)  [Eq. 1]
- \( p = \frac{d}{2} + (m \times s) + (n \times w) + \frac{d}{2} \)  [Eq. 2]
- \( n = \text{Int}[\left(\frac{p - d - s}{w + s}\right)] \)  [Eq. 3]

**Table of “n” for Different Minimum Feature Sizes**

<table>
<thead>
<tr>
<th>Ball Pitch</th>
<th>Line &amp; Space (minimum feature size, s and w)</th>
<th>Routing Layers Required</th>
<th># of Lines (between pads, n)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.5 mm</td>
<td>75 µm</td>
<td>12*</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>50µm</td>
<td>6</td>
<td>2</td>
</tr>
<tr>
<td></td>
<td>35µm</td>
<td>4</td>
<td>3</td>
</tr>
<tr>
<td></td>
<td>28µm</td>
<td>3</td>
<td>4</td>
</tr>
<tr>
<td></td>
<td>19µm</td>
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<td>6</td>
</tr>
<tr>
<td></td>
<td>10µm</td>
<td>1</td>
<td>12</td>
</tr>
</tbody>
</table>

**Notes:**
1) * = starting assumption
2) \( \therefore [R.L.R. * (# Lines)] = \) constant; 12 in this example
3) white rows – see next pages
BGA Land Pattern, 50x50 BGA Grid, 100 μm-Line Pitch

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## BGA Land Pattern, 50x50 BGA Grid, 38 µm-Line Pitch

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Routing More Lines Between Pads

By decreasing linewidths:

- Can route more traces through a BGA
- This reduces the # of routing layers
- Compare SAP and SE for # of lines between pads
  - SE upper limit is about 1 trace
  - SAP upper limit: photolithography limited
Benefits of using SAP Technology in PCB Designs

- Increase # of traces through BGA
- Reduce # of:
  - layers in PCB
  - laminations
  - microvias
- Combined, these promote:
  - decreased board size
  - higher reliability
  - lower costs
  - smaller environmental footprint
- Can design with much:
  - shorter line lengths
  - thinner dielectrics
  - thicker dielectrics (& use tightly-coupled differential conductor pairs)
- Could combine low-density SE layers with high-density SAP layers in one board design
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Specific Circuit Application Example: DDR4 S

- DDR4 SODIMM reference design (above)
- Multi-layer CAD drawings (at left)
  - Upper drawing: original reference design, 75 um lines and spaces for SE Process
  - Lower drawing: re-design, using SAP design guidelines, 35 um line & 52.5 um space

(Courtesy, T. Chester, Ref. [3] & Altium)

Notes:
(1) SODIMM (or SO-DIMM): Small Outline Dual In-Line Memory Module
(2) DDR4: Double Data Rate 4
(3) e.g., https://resources.altium.com/p/fly-topology-routing-ddr3-and-ddr4-memory
Specific Example: DDR4 SODIMM (cont’d.)

- Same circuit
- Focus: Signal Layer around BGA land pattern, single metal layer views

- *Upper drawing*: original design 75 um lines and spaces for SE. One or two lines fit.

- *Lower drawing*: SAP version of the same circuit. Up to four lines run between pads.

(Courtesy, T. Chester, Ref. [3] & Altium)
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Considerations

- Look at joining finer lines at the BGA to wider lines outside.

- Board designs typically use a Characteristic Impedance of $Z_0 = 50$ Ohm for signal lines.

- However, when signals meet mismatched impedances, reflections result & can distort the signal.

- Signal Integrity (SI): potential signal distortion = $f$(impedance, line length, slew rate, etc.)

Refs. [5 – 7]
Impedance Variation

- Q1. Why \(Z_0 = 50\) Ohms?  
  A1. This is a practical but arbitrarily-chosen standard value. Often, Integrated Circuit I/O’s are designed to it.

- Q2. Where does \(Z_0 \neq 50\) Ohms?  
  A2. Generally, where a metal line cross-section changes*

- Q3. Why?  
  A3. By (i) design or (ii) through manufacturing process variation

- Q4. When does it matter?  
  A4. When good Signal Integrity (SI) becomes critical

- Q5. How much?  
  A5. Today, +/- 10% \(Z_0\) tolerance is accepted. Too often, it can’t be achieved. Moreover, we see this spec tightening into the future.

Note: * – other factors also apply. See, e.g. Refs. [5 – 6]
Two Sources of Impedance Variations due to Widths

- **Manufacturing Process Variations** in width
  - From process variation: across a panel, within a batch, batch-to-batch, etc.
  - Impedance ($Z_0$) change: $Z_0 \uparrow$ as line width $\downarrow$ (see next slide)
  - Possible Signal Integrity (SI) degradation if I.C.’s $Z_0$ not matched to line’s $Z_0$
  - However, there is less process variation with SAP compared to SE

- **Intentional Design Changes** in width
  - Uneven-size metal lines joined by design (e.g. route lines away from BGA)
  - Signal reflections may occur any time there is impedance mismatch
  - Reflection magnitude depends on many factors
    - Q. Are the reflections significant?
    - A. Must do SI analysis (line length, signal slew rate, etc.)
Impedance Changes from Process Variations

- **Microstrip transmission line**
- **Assume:**
  - one 10 mil-wide trace (250 um)
  - 5 mil-thick dielectric
  - Dk = 4.0
  - ground plane beneath
- **Variations:**
  Processing Width
- Calculate the impedance, $Z_0$, as line width changes

[7]
Effects of Line Width Changes (cont’d.)

- Tighter manufacturing tolerance on linewidth with SAP gives tighter $Z_0$ than with SE

- Intentional width changes by design, such as during PCB layout (e.g., routing out of BGA)
  - Even more dramatic $DZ_0$, compared to manufacturing process

- Impedance changes will result in reflections. The lengths of the lines also play a role

- Therefore, signal integrity must consider both effects
  (i) design
  (ii) process
Conclusions

- We’ve demonstrated a SAP PCB layout on the signal layer of a DDR4 SODIMM circuit

- SAP
  - minimizes line widths and their processing variations
    - allows more lines between BGA for many benefits
    - fewer layers, laminations, and microvias
    - …resulting in lower production costs and higher reliability
    - worth pursuing, especially for designs with large BGA pad counts
  - SAP layers may be combined with SE layers in the same board

- Proper routing requires careful considerations of signal integrity
Acknowledgements

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▪ Eric Bogatin and students / CU Boulder: signal integrity
Please Look for This Upcoming Paper

E. Bogatin, C. Suresh, M. Piket-May, Univ. of Colorado,
and H. Basit, P. Dennig, Averatek Corp., “Utilizing Fine Line PCBs with High Density BGAs,”
*Signal Integrity Journal* [manuscript submitted for publication]. To be available:

https://www.signalintegrityjournal.com
References

[1] https://www.jedec.org/standards-documents/docs/dg-414h, see, for example, “DESIGN REQUIREMENTS FOR OUTLINES OF SOLID STATE AND RELATED PRODUCTS / Ball Grid Array Package and Interstitial Ball Grid Array Package,” publication JEP95.


