Semi-Additive PCB Processing: Process, Reliability Testing and Applications

Mike Vinson, Averatek, Santa Clara, CA

Abstract

The continued miniaturization of both packaging and component size in next-generation electronics presents a significant challenge for PCB designers and PCB fabricators. To effectively navigate the constraints of the traditional subtractive-etch PCB fabrication processes, PCB designs require advanced PCB fabrication capabilities pushing the limits of finer feature size, higher layer counts, multiple levels of stacked microvias and increased lamination cycles. Semi-Additive PCB processes, which can be implemented and integrated with existing PCB fabrication equipment and processes, provide an alternative that effectively resets the SWaP-C curve while increasing reliability.

The ability to design with and manufacture a 15-micron trace and space repeatedly and reliably provides options and opportunities previously not available to PCB designers and PCB fabricators. While just scratching the surface, Semi-Additive PCB processes can:

- reduce the number of layers needed for routing high density BGA's
- increase the hole size
- reduce the number of microvia layers required
- dramatically reduce size, weight and packaging and conversely increase the electronic content within an existing footprint

These benefits and more are being explored and realized as PCB fabricators implement semi-additive processes into their manufacturing facilities.

This session will begin with an overview of Semi-Additive technology as it relates to PCB fabrication including materials, equipment required, and process flow. This overview will be followed by a discussion of reliability test results and signal integrity modeling and will close with the discussion of use cases demonstrating the various ways the technology can be applied.

Introduction

Recent studies indicate the market is still strong in the HDI, SLP, and advanced substrate markets. COVID-19 has slowed down some sectors but accelerated and revived others. Telecommuting and video conferencing have become common place and the hardware necessary to effectively take advantage of these has led to an increase in personal computing beyond previous expectations. 5G and AI are driving infrastructure changes that, while slightly slowed, are moving forward this year.

A-SAP™ differentiates itself form other Semi-Additive processes by producing an extremely thin electroless layer of copper that will promote optimized circuit formation for low-loss high-frequency solutions. The value proposition we will be discussing here is not purely technical. Ease of adoption, manufacturability, and availability of supporting tools all go into the success of any incremental change.

Methodology

A-SAP™ is a Semi-Additive technology that does not depend on expensive materials that may be in short supply or regionally restricted. The standard PCB shop in North America, Europe and certain parts of Asia may have problems acquiring the necessary components to implement competitive technologies, however all the process steps with A-SAP™ can be acquired locally with only minor changes to the infrastructure used today. This low infrastructure cost will create an additional advantage in the capability of the A-SAP™ process. (Figure 1)

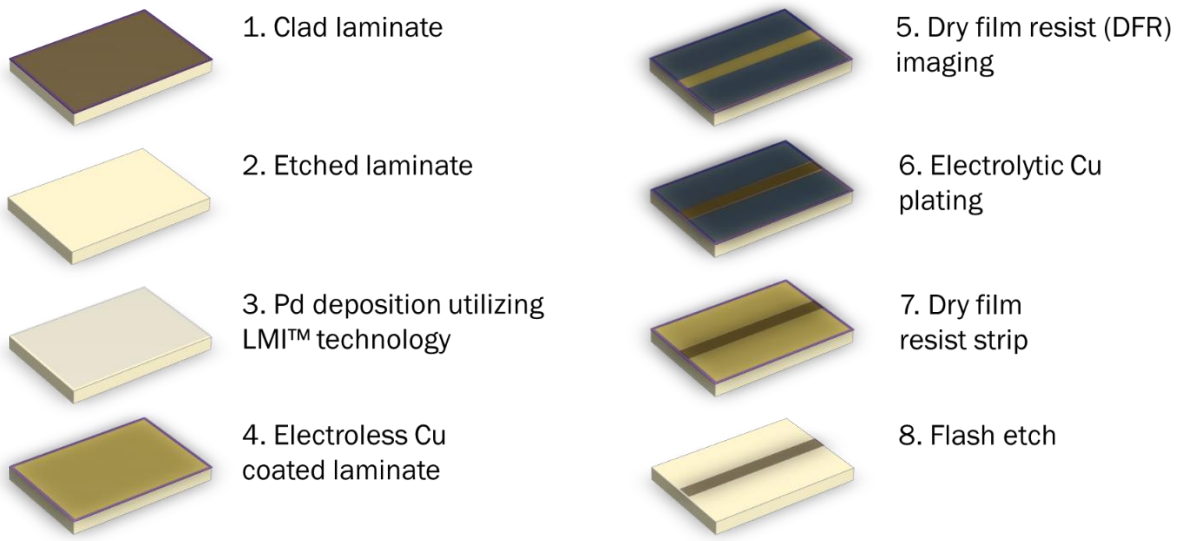


Figure 1- Averatek Semi-Additive Process (A-SAP™)

The process deposits a thin dense palladium layer, which is only nanometers thick and is largely transparent both visually and electrically. This is a result of the LMI™ (ink) and subsequent palladium layer which can penetrate the finest features, creating a coating that is both uniform and dense. These few simple steps are the only additional process requirements in the fine line factory implementing A-

SAP™ enabled products. The density of the base copper layer and the types of circuits it supports will be the main topic of this white paper.

Background

The thin layer of Pd is often hard to detect, with the best detection method being plating with electroless copper. The following test illustrates the thin dense nature of the ink, but a thicker layer than normal was used to be detectable in the transmission electron microscope (TEM), shown in Figure 2.

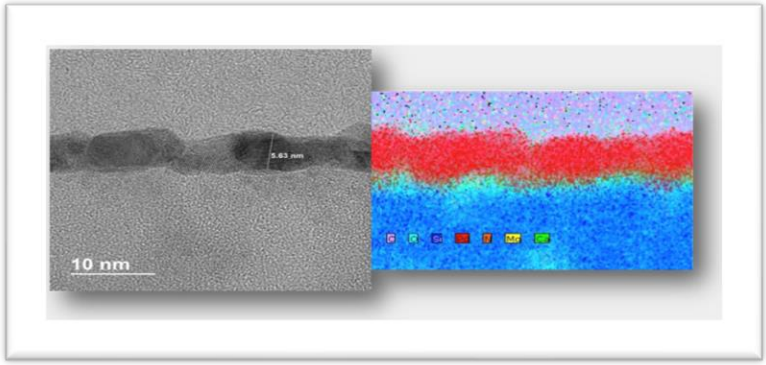


Figure 2- Thin palladium layer shown in a side view in red

This example structure was made on a glass sheet with the silicon layer below and the carbon layer above. The 5 to 6 nm palladium layer is still very conformal to the surface of the glass. Normally in PCB manufacturing the layer is ~2 nm thick, which is barely perceptible.
When used to support thin copper plating using the A-SAP™ process, the dense ink allows us to apply a sub-micron thickness of electroless copper, usually 200 to 400 nm, that gives us a base for copper electro plating of the traces.

Figure 3 shows an example of the A-SAP™ method. The conformal nature of the base copper provides for several manufacturing advantages. The ability to penetrate the cavities in the surface even beyond the line of sight is a distinct advantage over other thin coating methods such as sputtering. In other words, there's no shadowing. Some applications require finer features on the sides of the trace including the bottom. A very fine topography of the surface can easily be processed and will have some advantages for high-frequency circuits, but the lower-cost rougher substrates are more suitable for most applications and can be easily processed as shown here.

Figure 3- Thin electroless copper base with electroplated trace and etched A-SAP finished trace

Data

Standard short and wide traces will be easy to build but provide very poor mutual inductance. The skin effect will limit the benefits of wider or thicker lines making it difficult to achieve small characteristic impedance. Conversely, high-aspect-ratio lines are traditionally more difficult to build but show excellent mutual inductance. The skin effect does NOT limit the benefit of thicker (taller) lines and is therefore easy to get small characteristic impedance values. Figure 4 compares these two approaches.

Figure 4- Standard versus high ratio conductors

The advantage can be seen in the coupling coefficient as shown in Figure 5

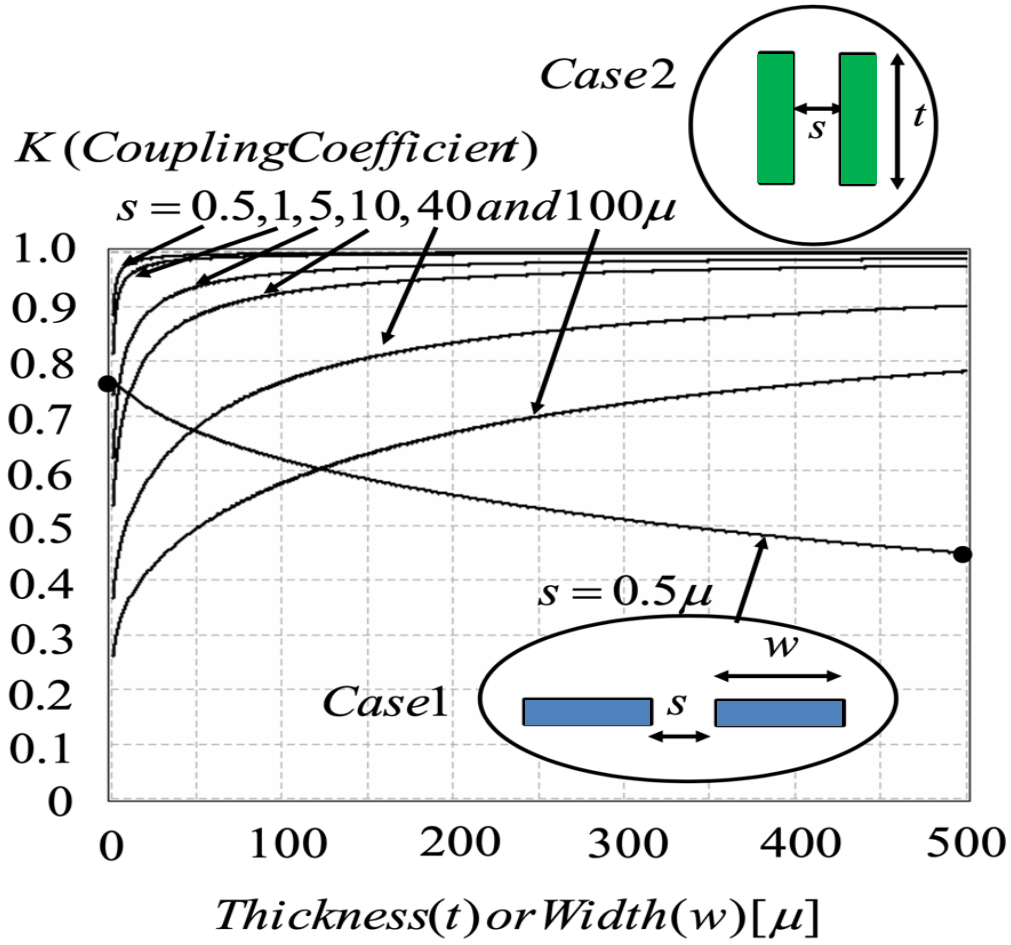


Figure 5 - Comparison of coupling coefficients

AirGuide™

Results

Microstrip, differential pairs and resonant structures were built to see what performance gains could be made by applying this technology. Representative high-speed structures were tested to confirm performance using available materials.

Testing on the microstrip features as built showed a 3% variance from the design parameters. This is much better than the 10% tolerance seen in Subtractive processing, allowing a better use of the overall design tolerance budget. Alignment with the glass weave was still a critical parameter on some materials which could add to the budget in special cases.

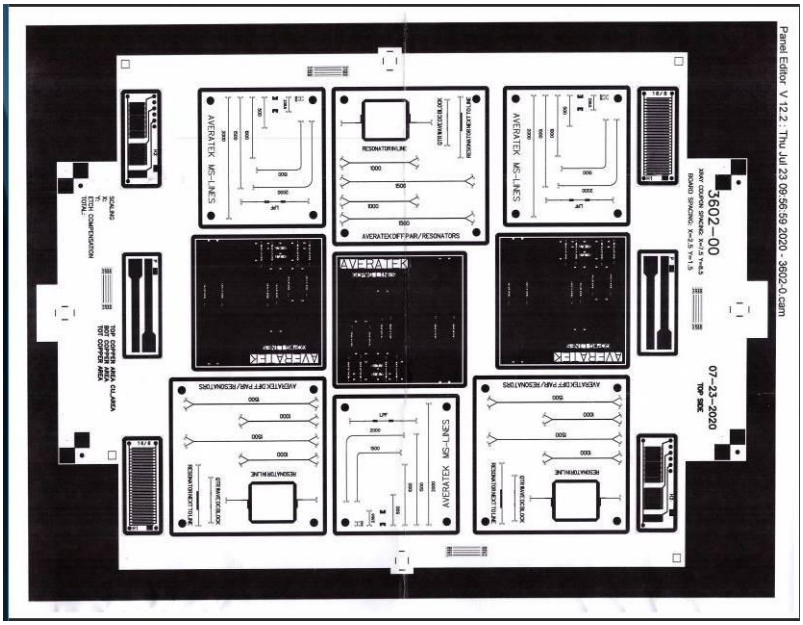
The Differential Pair Analysis likewise showed an improvement over the standard subtractive process. In a representative case, a 5.5% variance from the design parameters was observed and the result is much better than the 10% tolerance from subtractive circuit formation.

Resonance Structure Analysis

- The Microstrip Low Pass Filter had a 2.5% measurement error- noted as a very good first pass design
- The Simple Band Stop Filter had less than 0.5% error on the resonant frequency
- The Simple Interdigital ¼ Wave Series DC Series Block followed the simulation very closely

Table - Present materials being evaluated.

Material	Manufacturer	Type
370 HR	Isola	Standard FR4
P96	Isola	Polyimide
I-Speed	Isola	Mid-Loss
I-Tera MT40	Isola	Low-Loss
Tachyon100G	Isola	Low Loss
RO4350	Rogers	Low Loss
Megtron 6	Panasonic	Low Loss
R-F705S	Panasonic	LCP, Flex
N4800-20	AGC Nelco	Mid Loss
MW2000	AGC Nelco	Low Loss
MW4000	AGC Nelco	Low Loss
N4000-29	AGC Nelco	Standard FR4
N5000	AGC Nelco	BT
Pyralux AP	Dupont	Flex, Polyimide



Test pattern

Conclusion and summary

Subtractive methods where foil is etched away to form circuits are established processes that will continue for quite some time into the future but uses for this technique will be limited in the fast-growing High Density Interconnect (HDI) market where signal integrity is a key factor. A new leapfrog technology, A-SAP™, is available to accelerate the adaptation of miniaturized circuits optimized for high signal integrity through efficient methods and materials, requiring minimal investment in readily available equipment.

Some markets can tolerate the larger sizes and higher costs typically associated with the etching away of foil. The commercial-volume scale of smartphones and other system level PCB manufacturing is far less forgiving where costs and production efficiencies are concerned.

Acknowledgement

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